Using the Design for Six Sigma (DFSS) Approach to Design, Test, and Evaluate to Reduce Program Risk

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Agenda

- A Brief Six Sigma Primer
- The What and Why of Design for Six Sigma (DFSS)
- The DFSS Process

Six Sigma Defined

Originally: Metric Based on the Statistical Measure Called Standard Deviation

Expanded To:

WORLD CLASS QUALITY

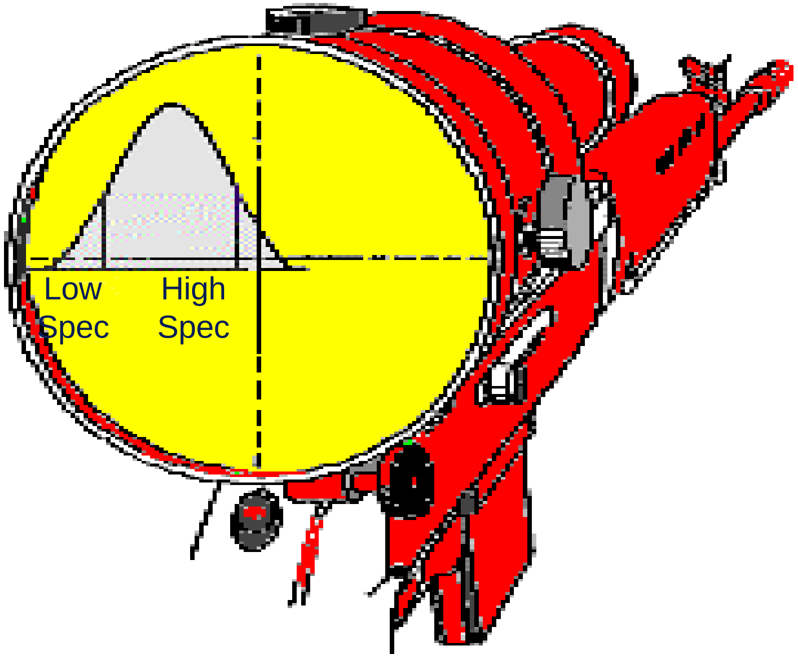
Providing a

BETTER product or service,

FASTER, and

at a LOWER COST

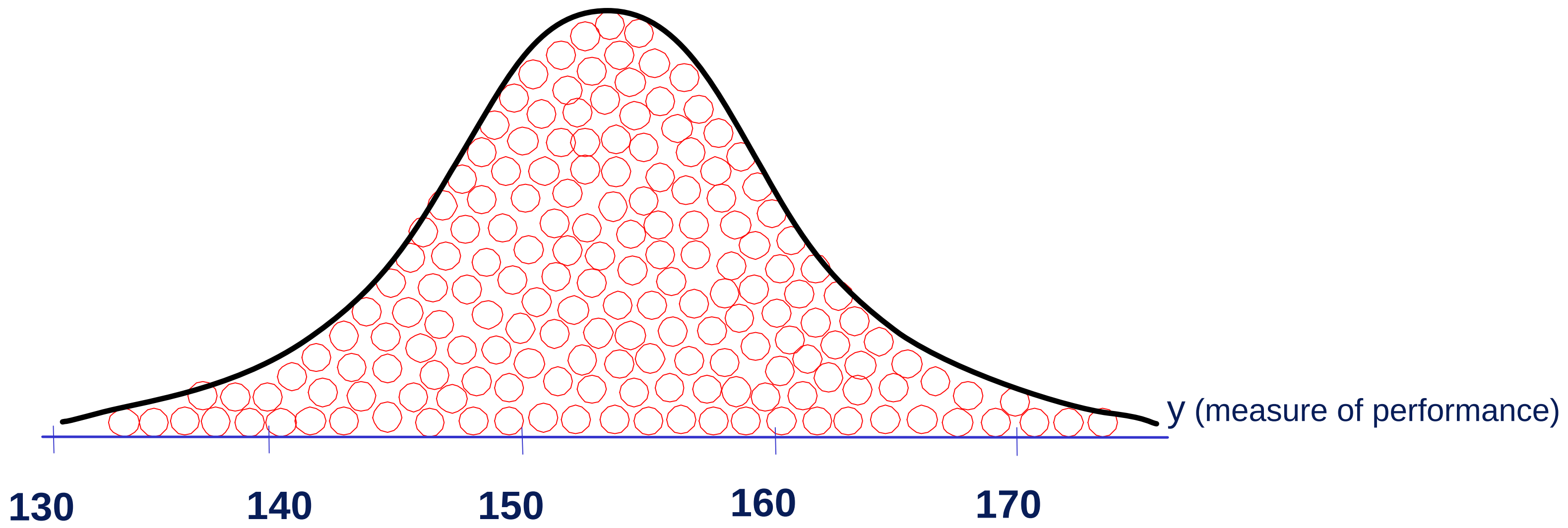
than our competition.



VARIATION is the enemy!

"*Always know the language of the enemy*."

Graphical Meaning of a Distribution



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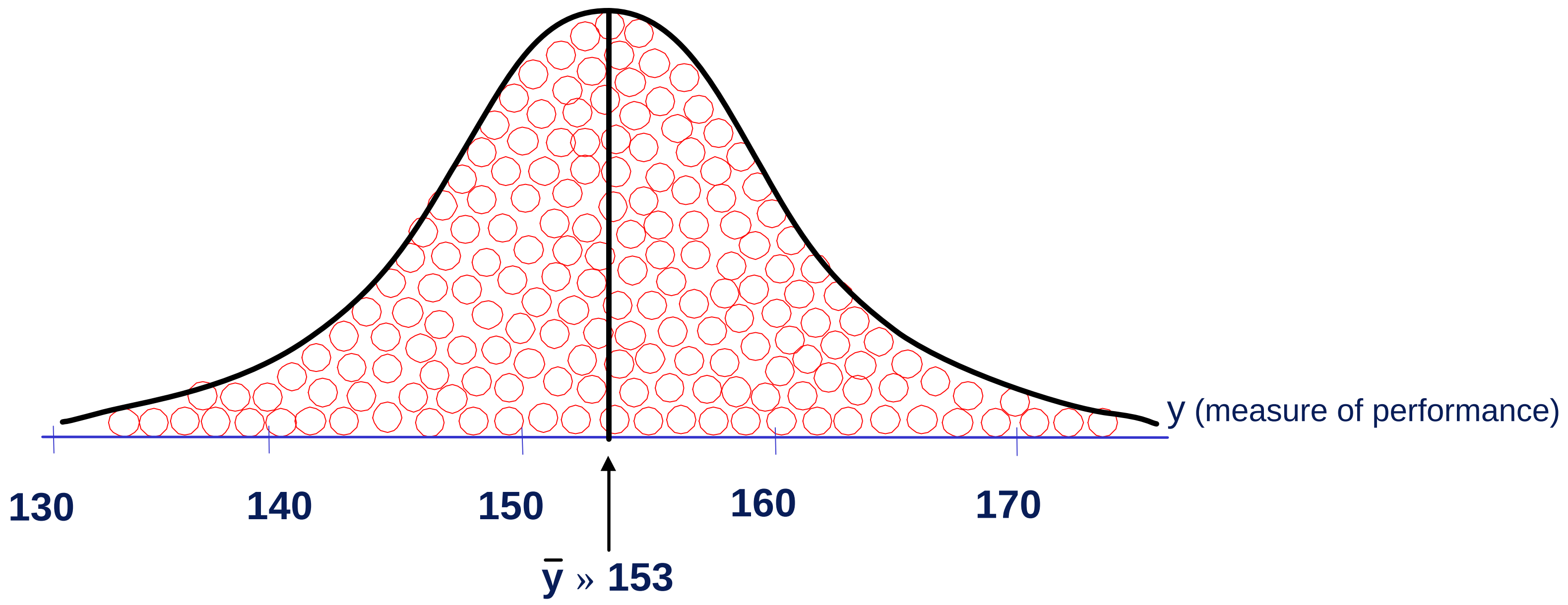
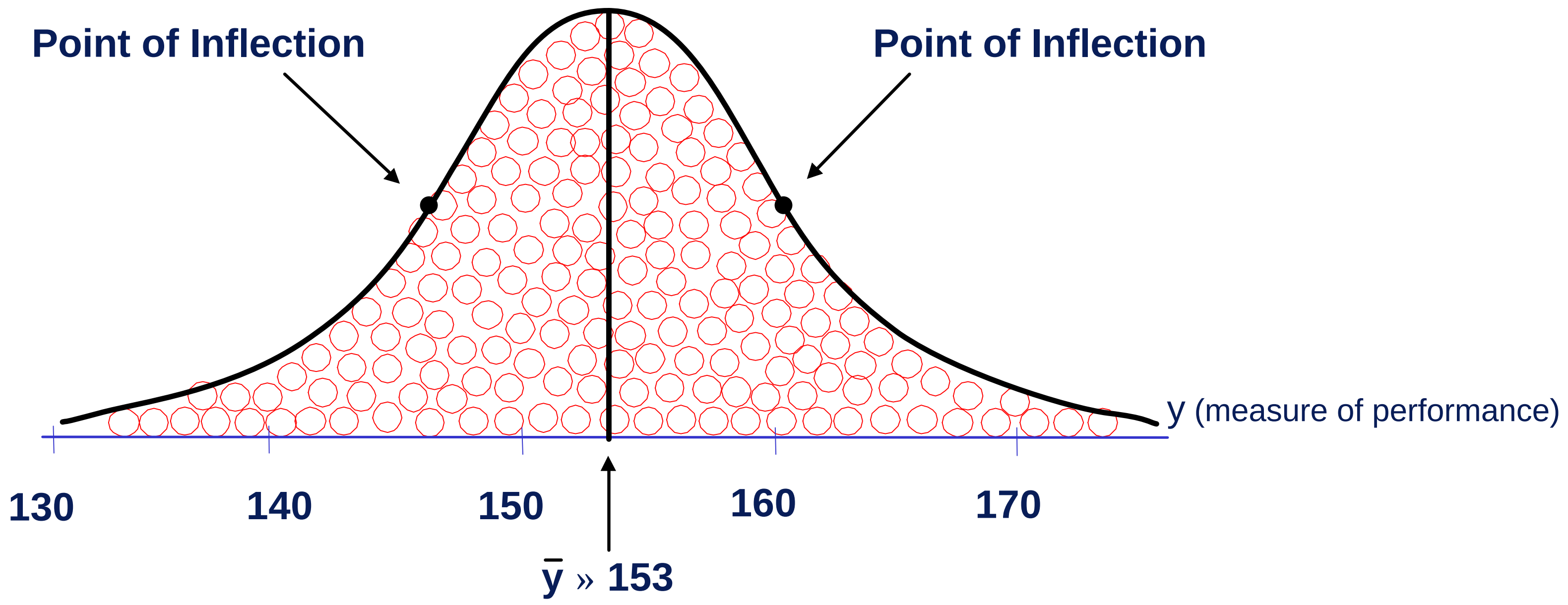
Graphical Meaning of $\bar{y}$

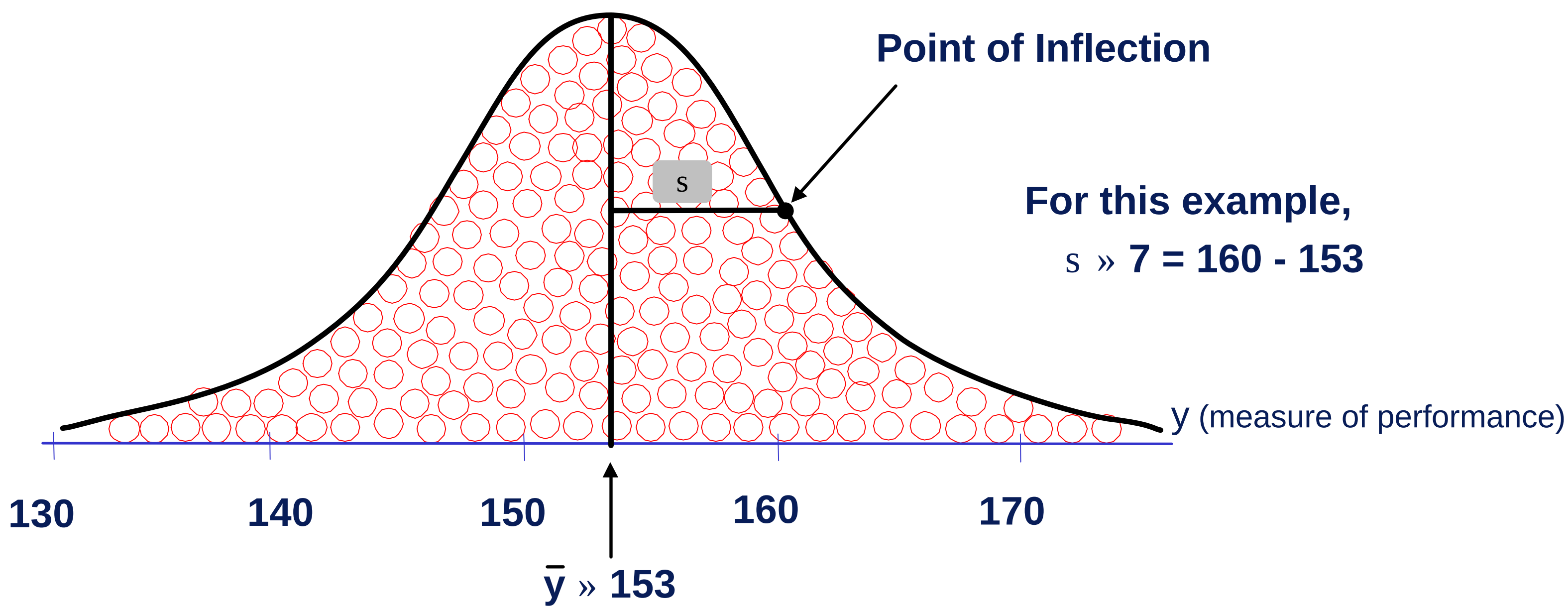


Graphical Meaning of Points of Inflection

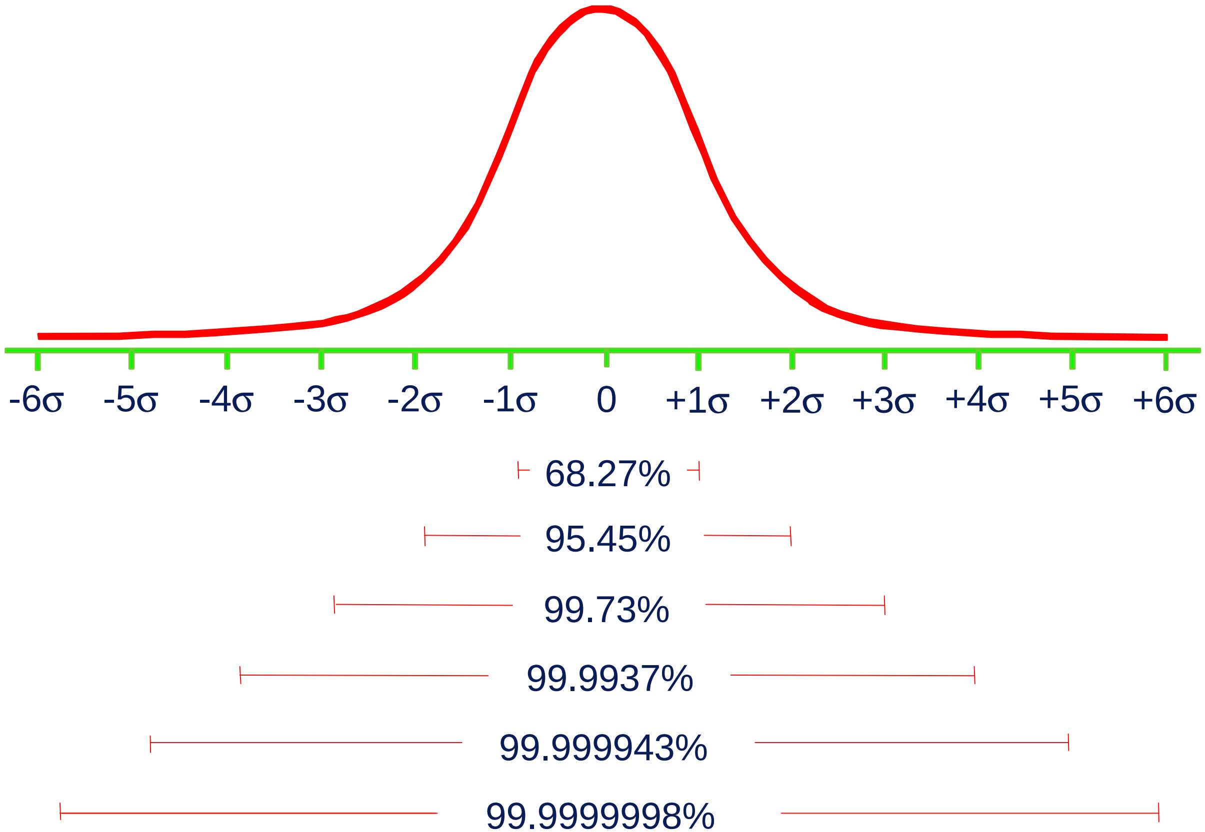


Graphical Meaning of s

s = distance from the center of the distribution to a point of inflection



Graphical View of Variation

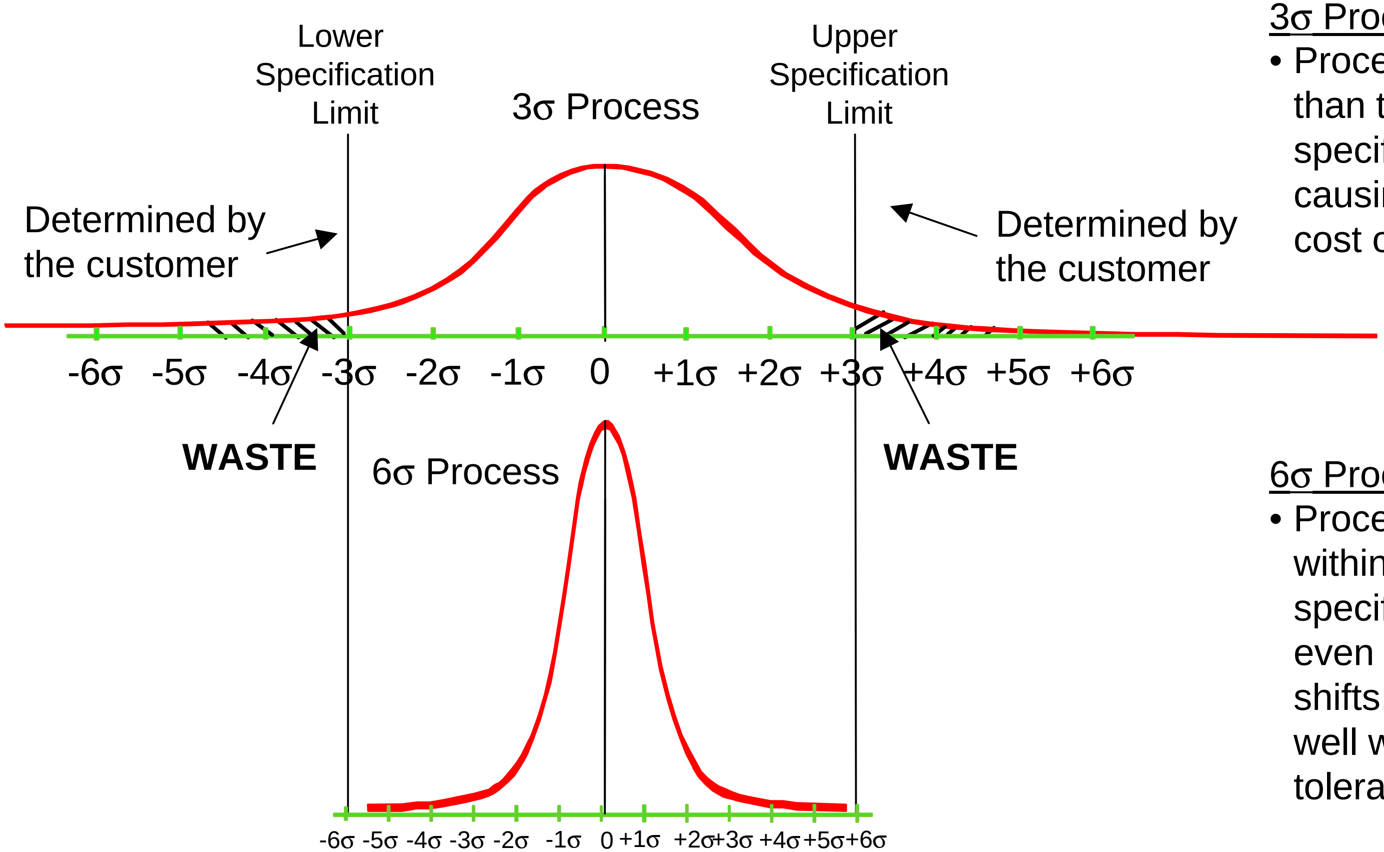


Typical Areas under the Normal Curve

Graphical View of Variation and Six Sigma Performance

The Sigma Capability of a process performance measure compares the Voice of the Process with the Voice of the Customer, and it is defined as follows:

The number of Sigmas between the center of a process performance measure distribution and the nearest specification limit



<u>3σ Process Centered</u>

- Process is WIDER than the specifications, causing waste and cost of poor quality

<u>6σ Process Centered</u>

- Process FITS well within the specifications, so even if the process shifts, the values fall well within tolerances

Six Sigma Measures Process Capability

<u>Sigma Capability</u> is a measure of process capability. It is correlated to the defect rate and the complexity of the process/product.

<u>Yield</u> is the probability that whatever we are producing (manufactured part, PO, shipped part, etc.) will pass through the entire process without rework and without defects.

σ Capability	DPMO	RTY
•	308,537	69.1%
•	66,807	93.3%
•	6,210	99.4%
•	233	99.97%
•	3.4	99.99966%

Process Capability	Defects per Million Opportunities	Rolled Throughput Yield

Six Sigma is a standard of Excellence.
It means less than 4 Defects per Million Opportunities.

Relationship Between Lean and Six Sigma

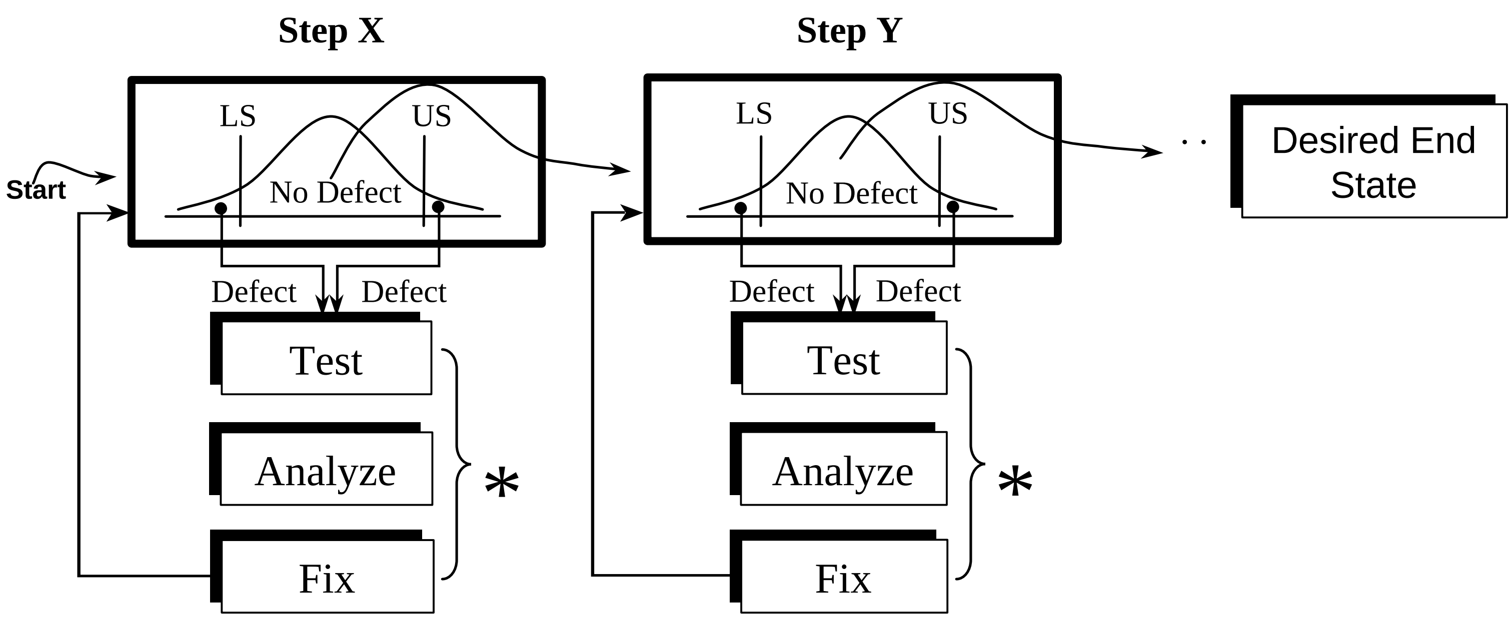
OVERALL YIELD vs SIGMA
(Distribution Shifted ±1.5σ)

# of Parts (Steps)	±3σ	±4σ	±5σ	±6σ
1	93.32%	99.379%	99.9767%	99.99966%
7	61.63	95.733	99.839	99.9976
10	50.08	93.96	99.768	99.9966
20	25.08	88.29	99.536	99.9932
40	6.29	77.94	99.074	99.9864
60	1.58	68.81	98.614	99.9796
80	0.40	60.75	98.156	99.9728
100	0.10	53.64	97.70	99.966
150	- - -	39.38	96.61	99.949
200	- - -	28.77	95.45	99.932
300	- - -	15.43	93.26	99.898
400	- - -	8.28	91.11	99.864
500	- - -	4.44	89.02	99.830
600	- - -	2.38	86.97	99.796
700	- - -	1.28	84.97	99.762
800	- - -	0.69	83.02	99.729
900	- - -	0.37	81.11	99.695
1000	- - -	0.20	79.24	99.661
1200	- - -	0.06	75.88	99.593
3000	- - -	- - -	50.15	98.985
17000	- - -	- - -	1.91	94.384
38000	- - -	- - -	0.01	87.880
70000				78.820
150000				60.000

Use for Benchmarking

Source: Six Sigma RESEARCH INSTITUTE
Motorola University Motorola, Inc.

How Process Capability Impacts Cycle Time and Resource Allocation



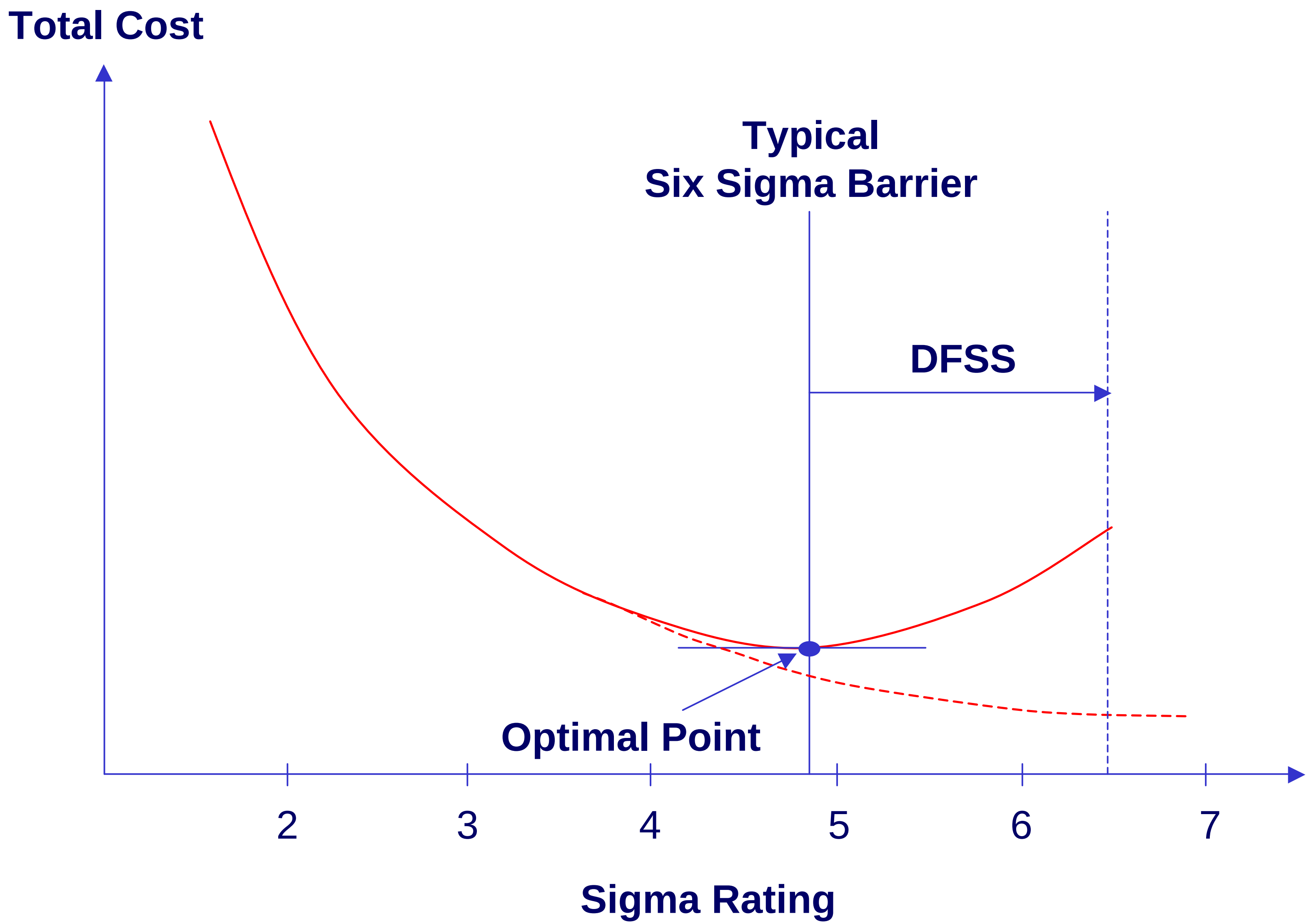
Every Time a Defect is Created During a Process (Step), it Takes Additional Cycle Time to Test, Analyze, and Fix.

* These Non-Value Added Activities Typically Require Additional Floor Space, Capital Equipment, Material, and People.

Six Sigma Project Phases

- **D** efine the problem / defects
- **M** easure the current performance level
- **A** nalyze to determine the root causes of the problem / defects
- **I** mprove by identifying and implementing solutions that eliminate root causes
- **C** ontrol by monitoring the performance of the improved process

What Have We Learned From Six Sigma?



Food for Thought...

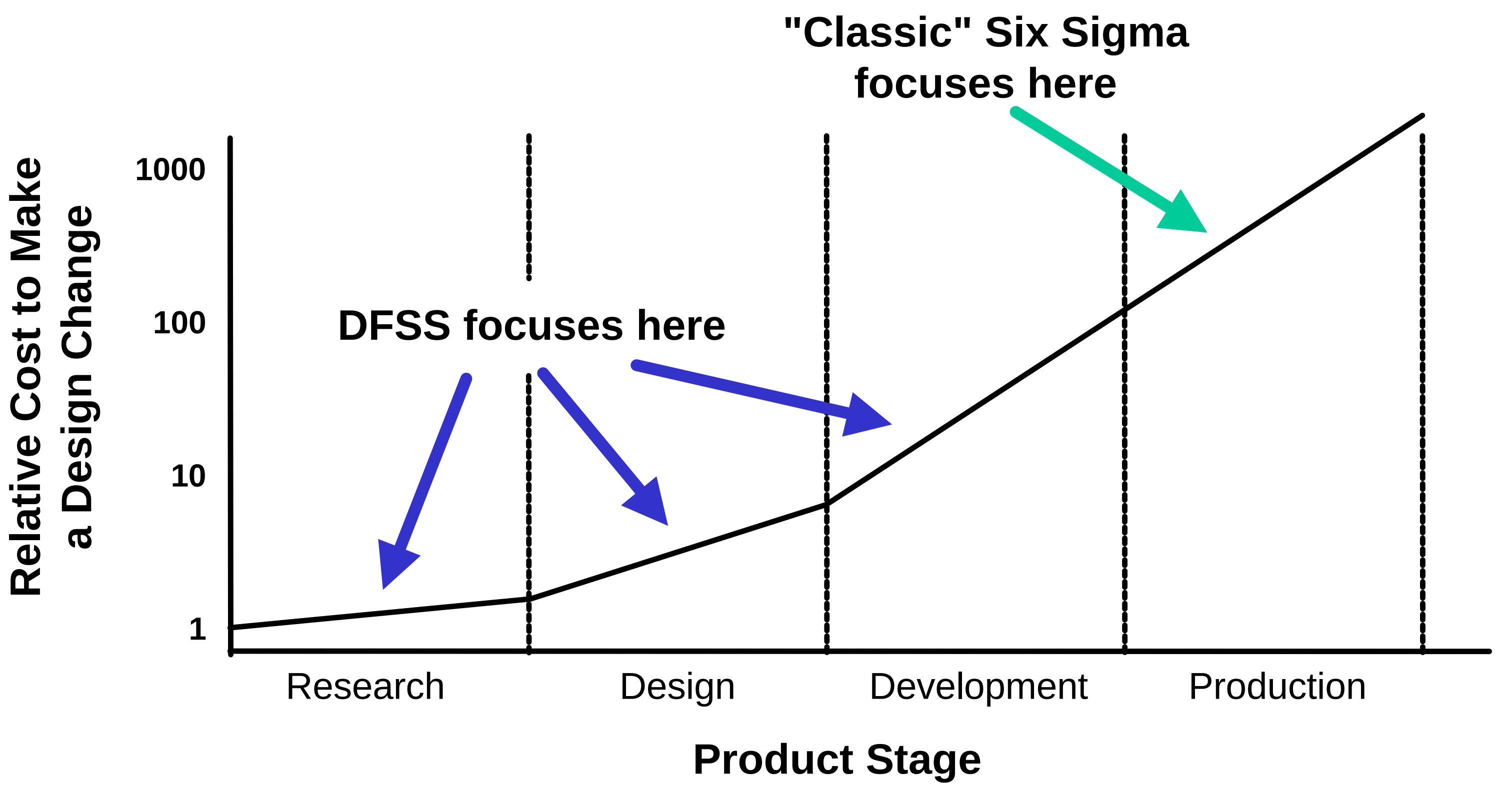
the systems and products that deliver value to our customers are perfectly designed to achieve the results we are getting today.

DFSS – What is it?

Design For Six Sigma is:

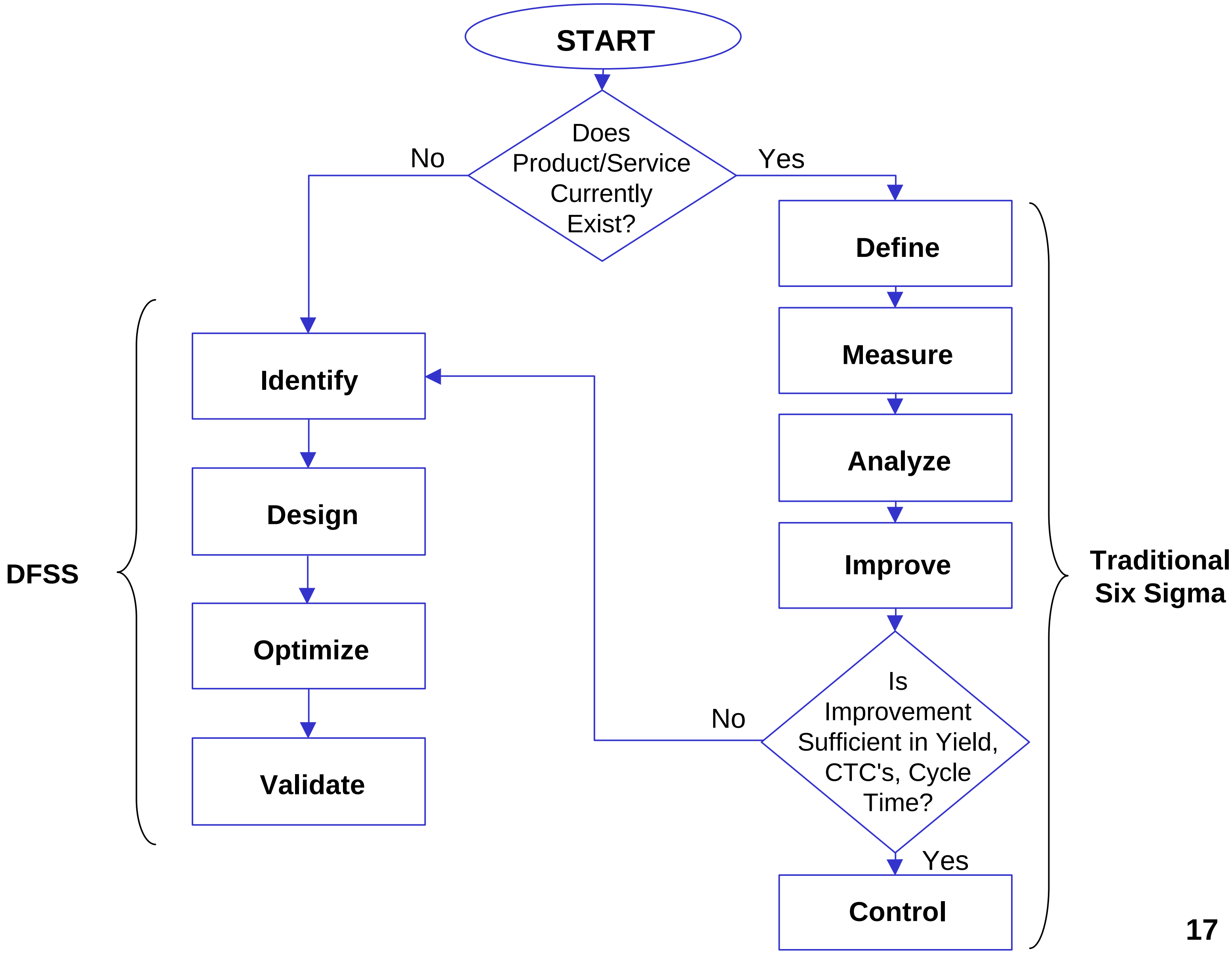
- A methodology for designing new products and/or processes.
- A methodology for re-designing existing products and/or processes.
- A way to implement the Six Sigma methodology as early in the product or service life cycle as possible.
- A way to exceed customer expectations.
- A way to gain market share.
- A strategy toward extraordinary ROI.

Why DFSS



- "Design in" quality when costs are lowest
- Show customers "Six Sigma" products right from the start

The Big Picture



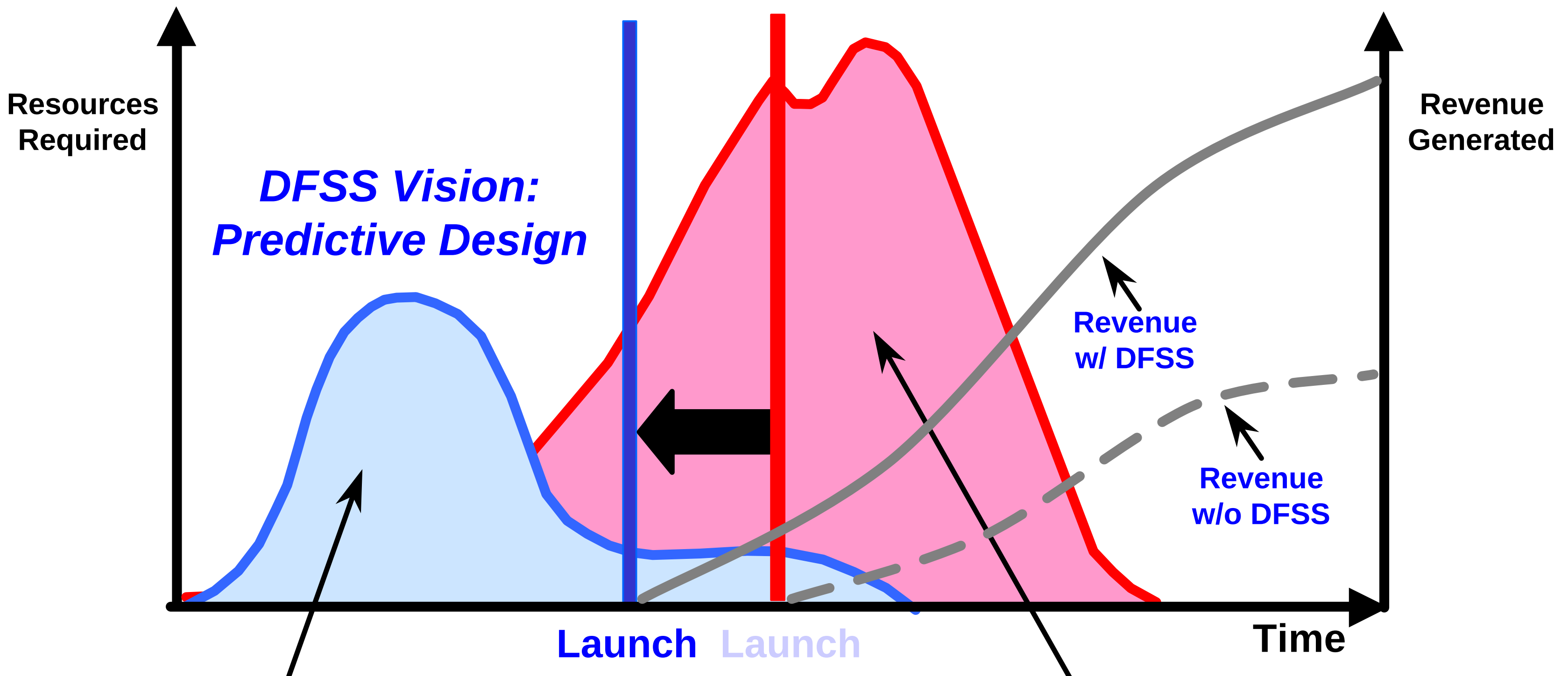
The Benefits of DFSS

- **Goal: Create new *game-changing* products and services which**
  - **Wow customers with *6σ performance* on their CTCs**
  - **Have *6σ reliability***
  - **Have *6σ manufacturability***
  - **Have *high performance/cost ratios***

- **Payoffs**
  - ***Quality designed in* from the start**
  - **Revenue *growth*: customer delight, market share, volume, price**
  - **Warranty cost reductions**

Driver for growth

The Opportunity of DFSS



- Early problem identification; solution when costs low
- Faster market entry: earlier revenue stream, longer patent coverage
- Lower total development cost
- Robust product at market entry: delighted customers
- Resources available for <u>next</u> game-changer

Pre-DFSS: Reactive Design

- Unhappy customers
- Unplanned resource drain
- Skyrocketing costs
- Next product compromised

- **Upfront investment is most effective and efficient**
- **Show customers "6s" products right from the start**

The Vision of DFSS

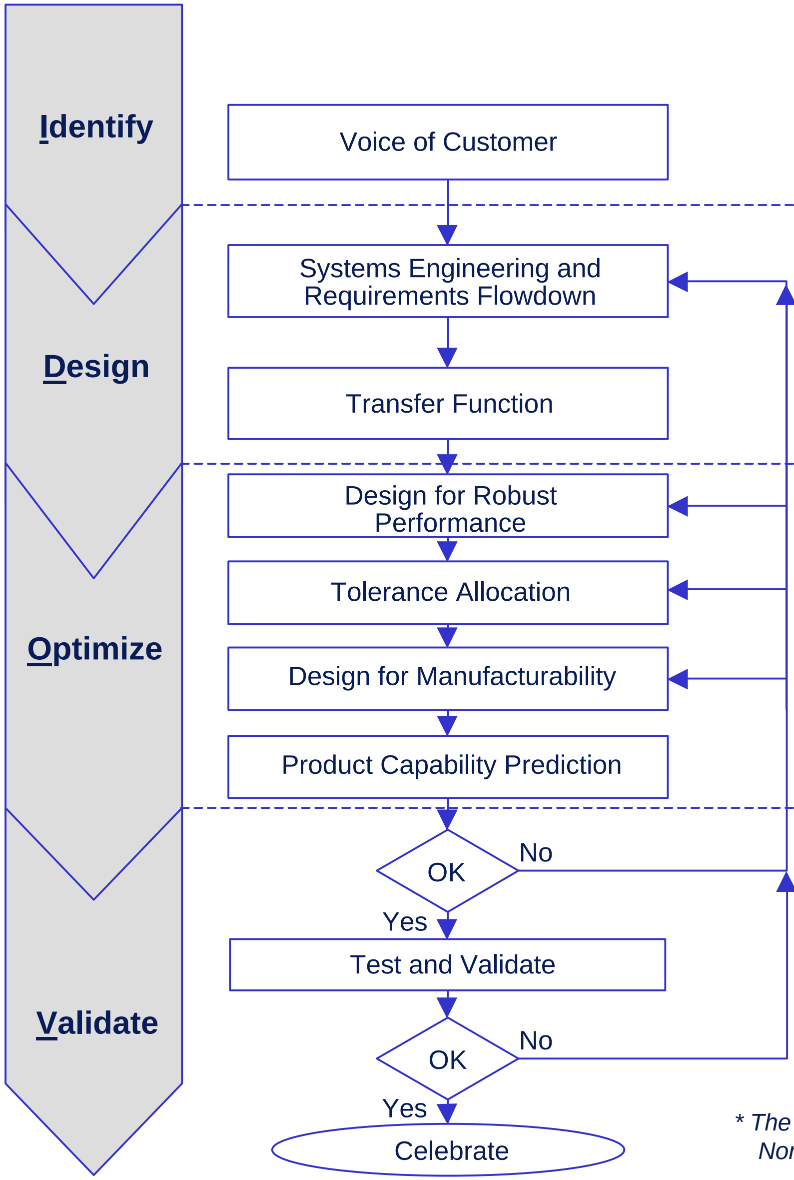
Reactive Design Quality → DFSS → Predictive Design Quality

From
- Evolving design requirements
- Extensive design rework
- Product performance assessed by "build and test"
- Performance and producibility problems fixed <u>after</u> product in use
- Quality "tested in"

To
- Disciplined CTC flowdown
- Controlled design parameters
- Product performance modeled and simulated
- <u>Designed</u> for robust performance and producibility
- Quality "designed in"

- 6 s products everywhere
- Revolutionize Engineering

DFSS Process



- Strategic Plan
- Benchmark Results
- Prioritized Customer Requirements
- Prioritized CTC's
- House of Quality #1
- Initial Performance Scorecard

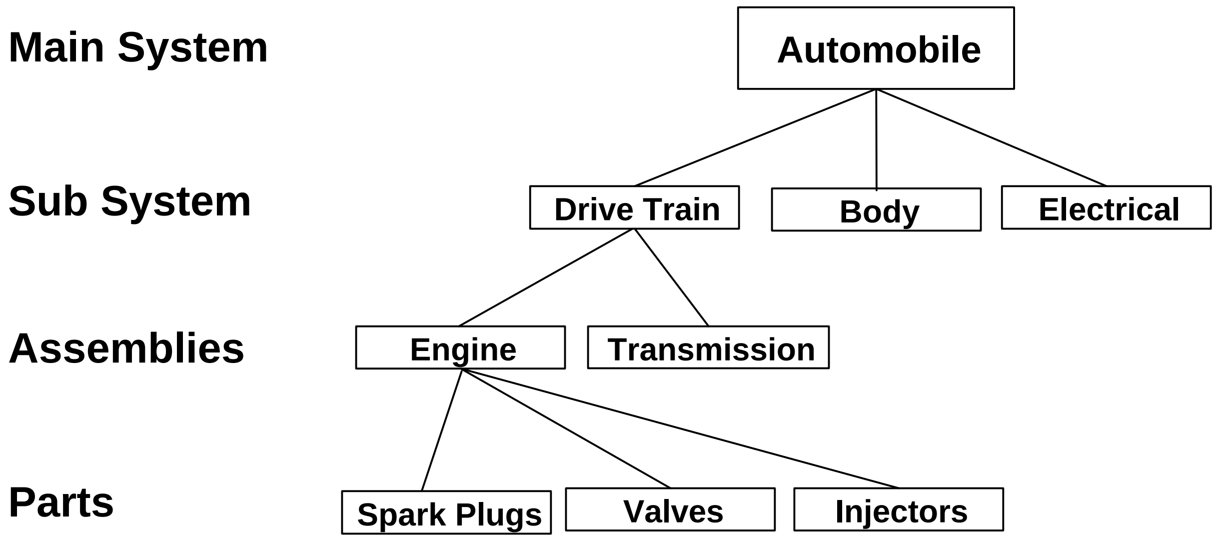
- For each CTC, Identify Design Parameters
- House of Quality #2
- Prioritized Product Design Characteristics
- Transfer Function(s)
- Preliminary Design Risk Assessment
- Performance/Process Scorecard

- Process Capability Studies
- Reliability Studies
- Capability Flowup
- Optimal Design
- Tolerances on X's
- Complete Scorecard

- Capable Product and Process
- Sensitivity Analysis
- Assess Performance, Reliability, and Risks

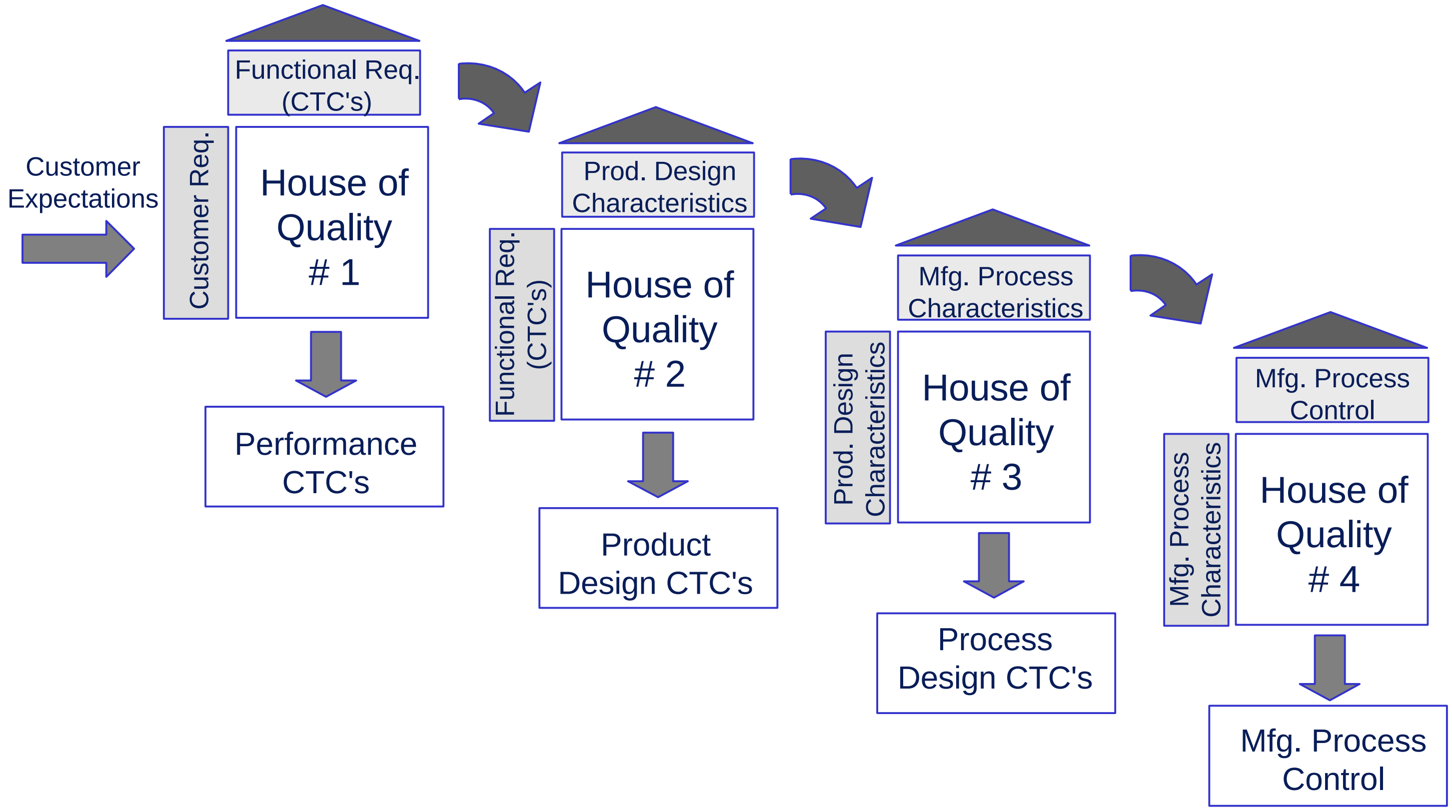
** The **IDOV** four-phase DFSS process originated with Dr. Norm Kuchar at GE CRD and is used with permission.*

Systems Engineering



- Complex products may require the "Divide and Conquer" approach.
- Flow the system requirements down and roll the capability up.
- System Engineers are the masters of the scorecard and make tradeoff decisions.

DFSS and Six Sigma



Marketing
- Features
- Quality
- Performance
- Cost

Design Engineering
- Performance
- Reliability
- Cost

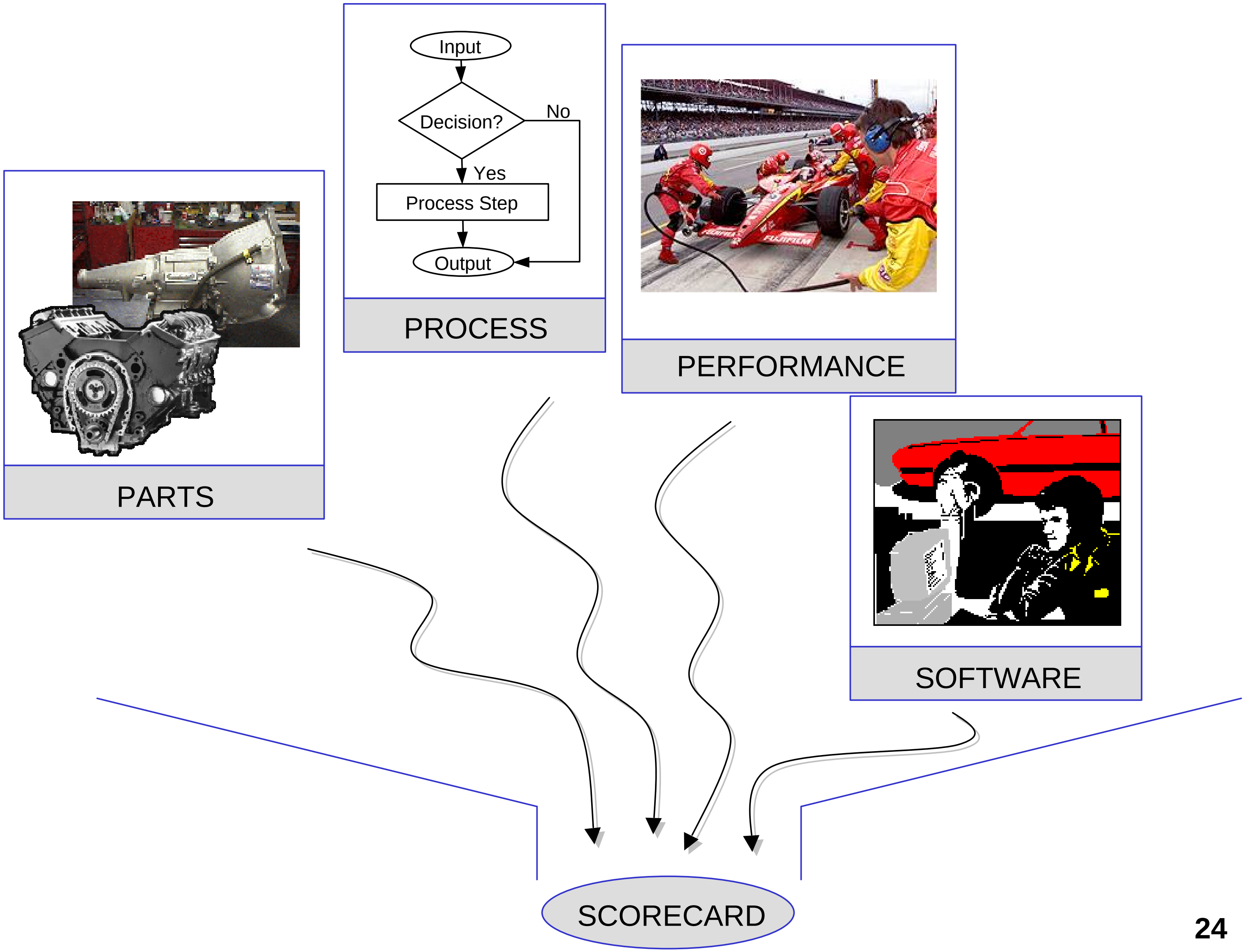
Mfg. Engineering
- Manufacturability
- Cost

Manufacturing
- SPC
- Process Capability

DFSS

Six Sigma

Scorecard Components



Scorecard Example

SOLENOID PART SCORECARD

#	Part Name	DPU	Qty	Continuous Variable Target	Mean	Std Dev	LSL	USL	UOM	Sample Size Known Sample Size	# Defective	ppm Only ppm
1	Wire	0.0000220	1									22
2	Power Supply	0.0008582	1	1.1	1.1	0.015	1.05	1.15	Amps			
3	Core (Length)	0.0000044	1	15	15	0.45	13	18	cm			
4	Core (Radius)	0.0008582	1	2	2	0.3	1	3	cm			
5												
6												
7												

SOLENOID PROCESS SCORECARD

#	Process Step	DPU	Qty	Continuous Variable Target	Mean	Std Dev	LSL	USL	UOM	Sample Size Known Sample Size	# Defective	ppm Only ppm
1	Apply Wire to Core	0.000063	1	110	110	1	106	114	Twist			
2	Attach Power Supply	0.000200	1							10000	2	
3												
4												
5												
6												

SOLENOID PERFORMANCE SCORECARD

#	Performance	DPU	Qty	Continuous Variable Target	Mean	Std Dev	LSL	USL	UOM	Sample Size Known Sample Size	# Defective	ppm Only ppm
1	Mag Force 4cm from center	0.0000921	1	7.5	7.47	0.254	6.5	8.5	Amp/cm			
2												
3												
4												

Solenoid Scorecard (cont.)

Scorecard Summary						
	# Steps/Parts	Total dpu	Yield	dpmo	ST Sigma	LT Sigma
Part	4	0.001743	99.826%	435.72	4.8289	3.3289
Process	2	0.000263	99.974%	131.69	5.1485	3.6485
Performance	1	0.000092	99.991%	92.12	5.2393	3.7393
Software						
Total	**7**	**0.002098363**	**99.790%**	**299.766**	**4.932**	**3.432**

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DFSS Tools

Identify

- Project Charter
- Strategic Plan
- Cross-Functional Team
- Voice of the Customer
- Benchmarking
- KANO's Model
- Questionnaires
- Focus Groups
- Interviews
- Internet Search
- Historical Data
- Quality Function Deployment
- Pairwise Comparison
- Design of Experiments
- Specify CTC's
- Performance Scorecard
- Flow Charts
- FMEA
- Visualization

Design

- Assign Specifications to CTC's
- Customer Interviews
- Formulate Design Concepts
- Pugh Concept Generation
- TRIZ or ASIT
- Pugh Concept Synthesis
- Controlled Convergence
- FMEA
- Fault Tree Analysis
- Brainstorming
- QFD
- Scorecard
- Transfer Function
- Design of Experiments
- Deterministic Simulators
- Confidence Intervals
- Hypothesis Testing
- MSA
- Computer Aided Design
- Computer Aided Engineering
- High Throughput Testing

Optimize

- Histogram
- Distributional Analysis
- Empirical Data Distribution
- Expected Value Analysis (EVA)
- Adding Noise to EVA
- Non-Normal Output Distributions
- Design of Experiments
- Multiple Response Optimization
- Robust Design Development
  - Using S-hat Model
  - Using Interaction Plots
  - Using Contour Plots
- Parameter Design
- Tolerance Allocation
- Reducing Standard Deviations of Inputs
- Design For Manufacturability
- Mistake Proofing
- Product Capability Prediction
- Part, Process, and SW Scorecard
- Risk Assessment
- Reliability
- Multidisciplinary Design Optimization (MDO)

Validate

- Sensitivity Analysis
- Gap Analysis
- FMEA
- Fault Tree Analysis
- Control Plan
- PF/CE/CNX/SOP
- Run/Control Charts
- Mistake Proofing
- MSA
- Reaction Plan

High Throughput Testing (HTT)

(for all two-way combinations)

Full Factorial = 8100 runs HTT = 27 runs

5 Levels **Motherboard**	*3 Levels* **Ram**	*3 Levels* **BIOS**	*3 Levels* **CD**	*5 Levels* **Monitor**	*3 Levels* **Printer**	*2 Levels* **Voltage**	*2 Levels* **Resolution**
Gateway	128 MB	Dell	Generic	Viewsonic	HP	220V	800 by 600
ASUS	256 MB	Award	Teac	Sony	Lexmark	110V	800 by 600
Micronics	512 MB	Dell	Sony	KDS	Cannon	110V	1024 by 768
Dell	128 MB	Generic	Teac	NEC	Lexmark	220V	1024 by 768
Compaq	256 MB	Generic	Sony	Generic	HP	110V	800 by 600
Dell	256 MB	Award	Generic	Viewsonic	Cannon	110V	1024 by 768
ASUS	512 MB	Award	Sony	Sony	HP	220V	1024 by 768
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Gateway	256 MB	Award	Teac	KDS	HP	220V	800 by 600
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Gateway	128 MB	Generic	Sony	Sony	Cannon	110V	1024 by 768
Dell	256 MB	Dell	Sony	NEC	HP	110V	800 by 600
ASUS	128 MB	Generic	Generic	KDS	Lexmark	110V	800 by 600
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Dell	512 MB	Generic	Teac	Sony	HP	110V	800 by 600
Gateway	512 MB	Award	Teac	NEC	Lexmark	110V	800 by 600
ASUS	128 MB	Award	Teac	Viewsonic	Cannon	110V	800 by 600
Compaq	128 MB	Award	Teac	Sony	HP	110V	800 by 600
Dell	128 MB	Award	Teac	KDS	HP	110V	800 by 600
ASUS	128 MB	Award	Teac	NEC	HP	110V	800 by 600
Dell	128 MB	Award	Teac	Generic	HP	110V	800 by 600
Micronics	128 MB	Award	Teac	NEC	HP	110V	800 by 600
Compaq	128 MB	Award	Teac	KDS	HP	110V	800 by 600
Gateway	128 MB	Award	Teac	Generic	HP	110V	800 by 600

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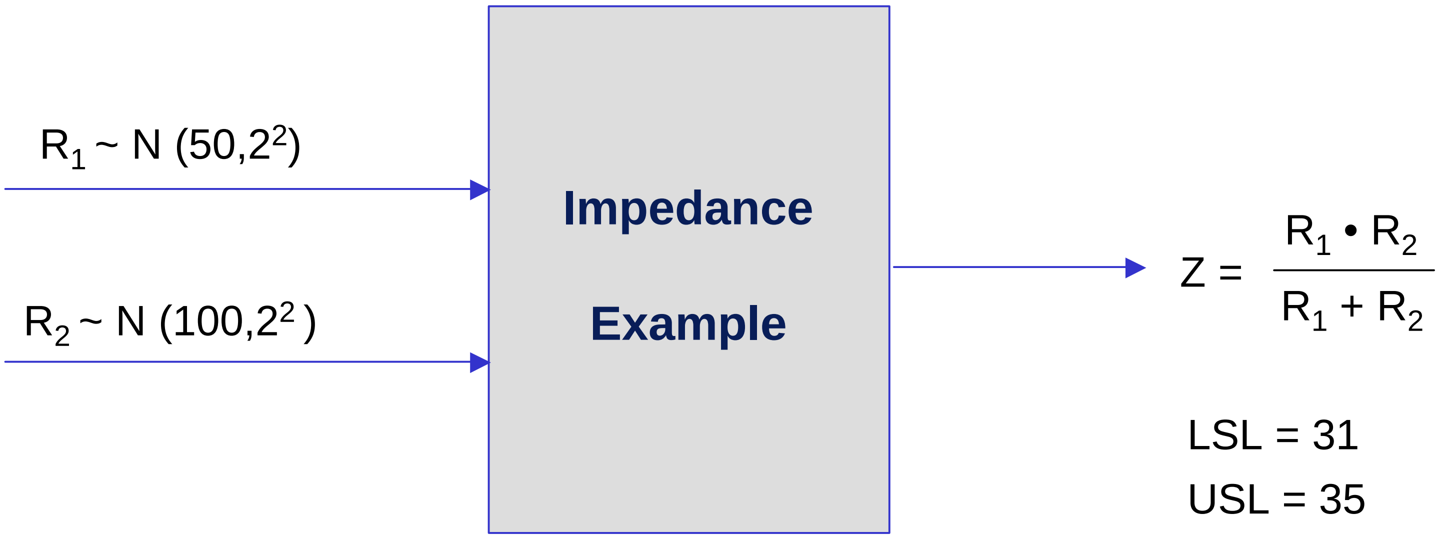
Tolerance Allocation Example



If we were able to change a resistor's standard deviation, which resistor, R_1 or R_2, would have the greater impact on the dpm of Z (impedance)?

Tolerance Allocation Example (cont.)

A reduction of R_1 by 50% reduces dpm by an order of magnitude X, while R_2 has little impact.

Tolerance Allocation Table N = 10,000 (in defects per million)		
Impedance Table		
	R1	**R2**
-50% Sigma	372.40	34,683
-25% Sigma	8,058	36,849
-10% Sigma	23,906	35,663
Nominal	39,220	39,657
+10% Sigma	59,508	37,556
+25% Sigma	92,398	47,317
+50% Sigma	148,113	46,801

A reduction of R_1's standard deviation by 50% combined with an increase in R_2's standard deviation by 50%

$$R_1 \sim N(50, 1^2)$$

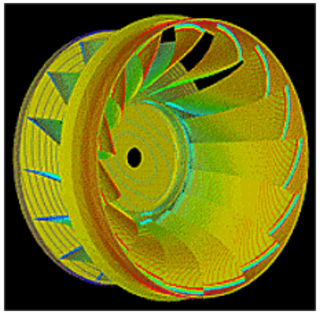
$$R_2 \sim N(100, 3^2)$$

results in a dpm = 1,254.

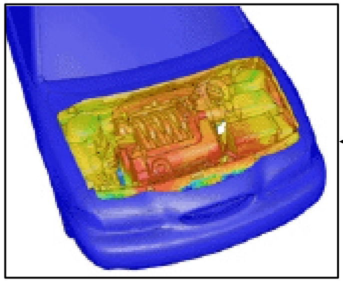
Examples of Simulation and High Performance Computing (HPC)

Power

Simulation of stress and vibrations of turbine assembly for use in nuclear power generation



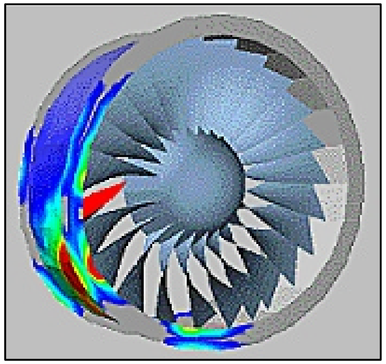
Automotive



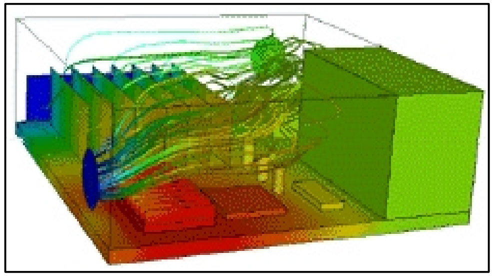
Simulation of underhood thermal cooling for decrease in engine space and increase in cabin space and comfort

Aerospace

Evaluation of dual bird-strike on aircraft engine nacelle for turbine blade containment studies



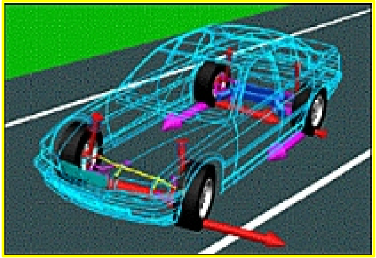
Electronics



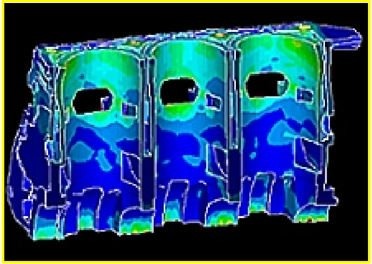
Evaluation of cooling air flow behavior inside a computer system chassis

Examples of Computer Aided Engineering (CAE) and Simulation Software

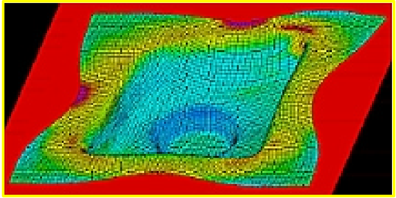
Mechanical motion: Multibody kinetics and dynamics
- ADAMS®
- DADS



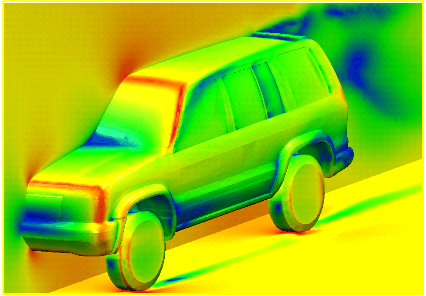
Implicit Finite Element Analysis: Linear and nonlinear statics, dynamic response
- MSC.Nastran™, MSC.Marc™
- ANSYS®
- Pro MECHANICA
- ABAQUS® Standard and Explicit
- ADINA



Explicit Finite Element Analysis : Impact simulation, metal forming
- LS-DYNA
- RADIOSS
- PAM-CRASH®, PAM-STAMP

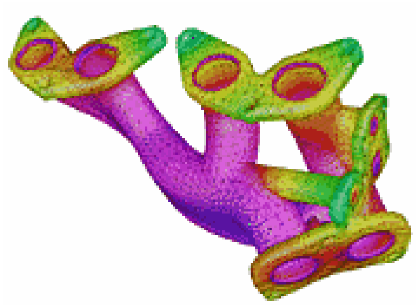


General Computational Fluid Dynamics: Internal and external flow simulation
- STAR-CD
- CFX-4, CFX-5
- FLUENT®, FIDAP™
- PowerFLOW®



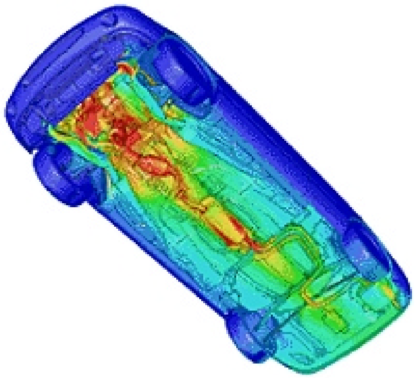
Examples of Computer Aided Engineering (CAE) and Simulation Software (cont.)

Preprocessing: Finite Element Analysis and Computational Fluid Dynamics mesh generation



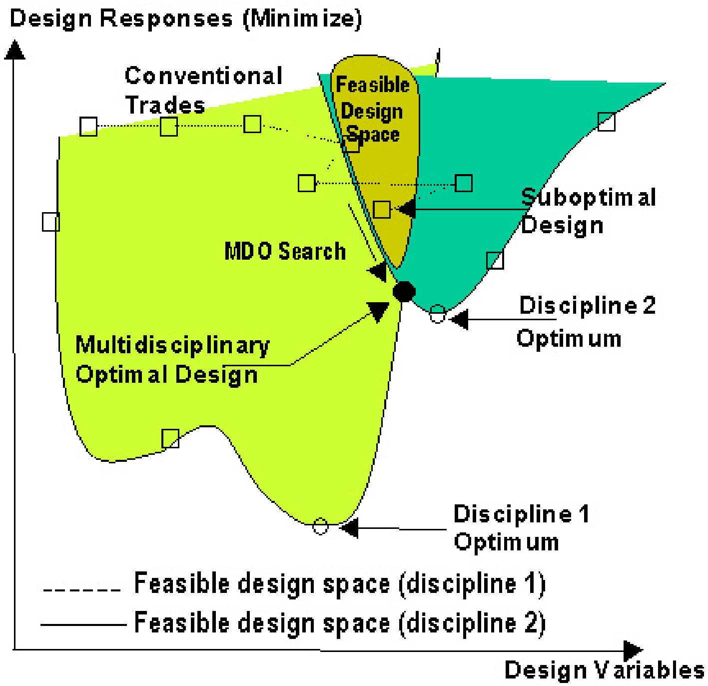
- ICEM-CFD
- Gridgen
- Altair® HyperMesh®
- I-deas®
- MSC.Patran
- TrueGrid®
- GridPro
- FEMB
- ANSA

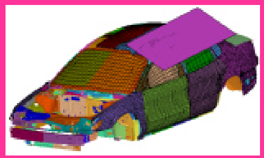
Postprocessing: Finite Element Analysis and Computational Fluid Dynamics results visualization



- Altair® HyperMesh®
- I-deas
- MSC.Patran
- FEMB
- EnSight
- FIELDVIEW
- ICEM CFD Visual3 2.0 (PVS)
- COVISE

Multidisciplinary Design Optimization (MDO): A Design Process Application





- CFD
- Structures
- Performance
- Controls
- Cost

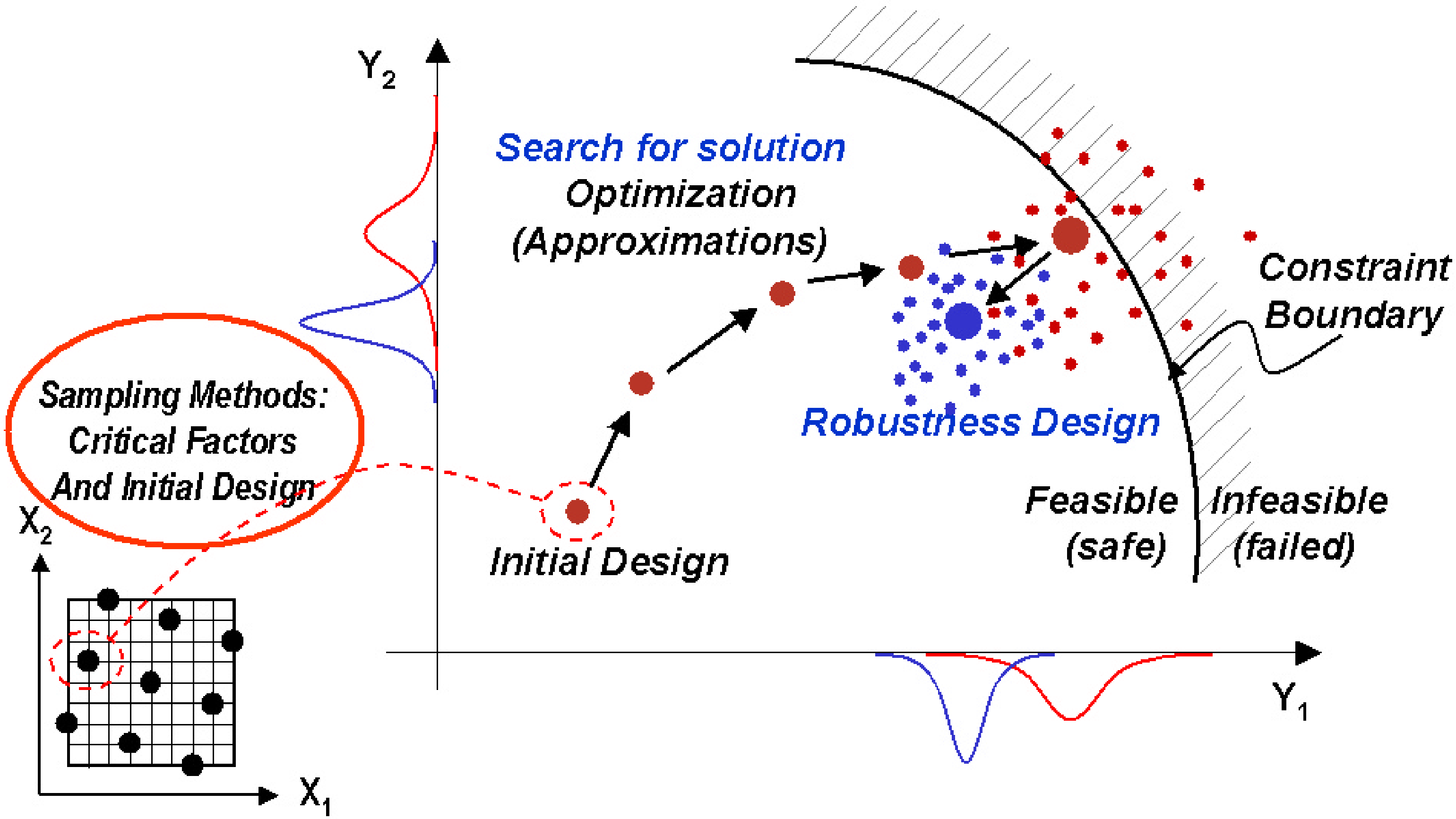
- NVH
- Safety
- Durability
- Controls Stability
- Cost

Key Elements of MDO

- Massive Computational Problem;
- Solution by decomposition effective for complex systems;
- Multiprocessor computing simplifies MDO solutions conceptually & enables solutions previously intractable;
- Aids in the management of the design process.

Mastery of interactions between the disciplines (or, subsystems) is as important as the methods & tools used within a single discipline

MDO: A Design Improvement Process



Environments Where MDO/HPC Is Beneficial

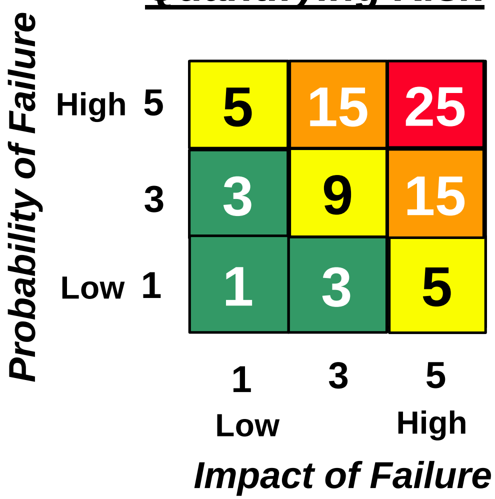
Design of complex vehicles & systems results in a simulation environment with:

- **A high number of design variables**
- **A substantial number of design subsystems and engineering disciplines**
- **Interdependency and interaction between the subsystems**
- **High resolution, complex models across several engineering disciplines**

Risk Assessment

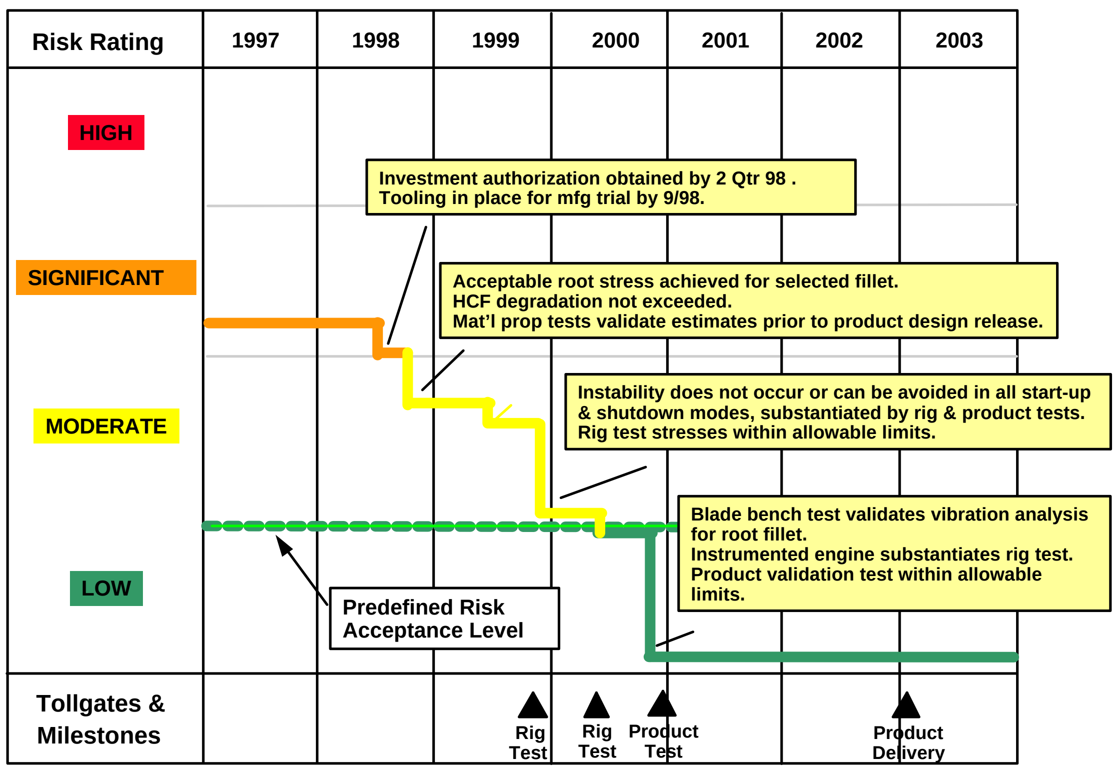
- Assess risks of key areas: technology, cost, schedule, market, etc.
- Use formal tools: FMEA, etc.
- Quantify risks: probability of failure and impact of failure
- Formulate responsive projects to reduce high risks
- Track progress with quantitative risk “waterfall”

Quantifying Risk



R Show stopper
O Significant risk
Y Fix before production
G Proceed with caution

Tracking Risk



Characteristics of a Successful DFSS Implementation

- **Commitment and leadership from the top**
- **Measurable, "stretch" goals for each project**
- **Accountability for project success**
- **Involvement and support of *everyone***
- **Training and implementing an extremely powerful, yet easy-to-use toolset for predicting quality and making tradeoffs before the product or process is even built**

> - **It's very easy to focus on the last item...**
> - **But, the first four – involving *leadership* and *cultural change* – are even more critical for success**