Cost Effectively Maintaining Legacy Systems Using GEM (Generalized Emulation of Microcircuits)

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Outline

- Emulation Program – Generalized Emulation of Microcircuits (GEM)
- Air Force B-1 Example
  - The Problem
  - Reverse Engineering
  - Generalized Emulation of Microcircuits (GEM) Solution
  - New Standard Microcircuit Drawing (SMD)
  - Conclusion

Microcircuit Emulation

… two decades of delivering military quality microcircuits …

- **Provide critical ICs no longer supplied by industry**
- **Reverse engineering, design, manufacturing and test of Military Quality Microcircuits which are …**
  - **Form**
    - **Same package, pin-out and marking**
  - **Fit**
    - **Same physical interface (footprint)**
  - **Function**
    - **Performs the same function and meets the electrical performance requirements of the required part specification**

… replacements for non-procurable item

- **End result – a part fully compliant and certified to the electrical, mechanical, quality and reliability criteria of the required microcircuit**

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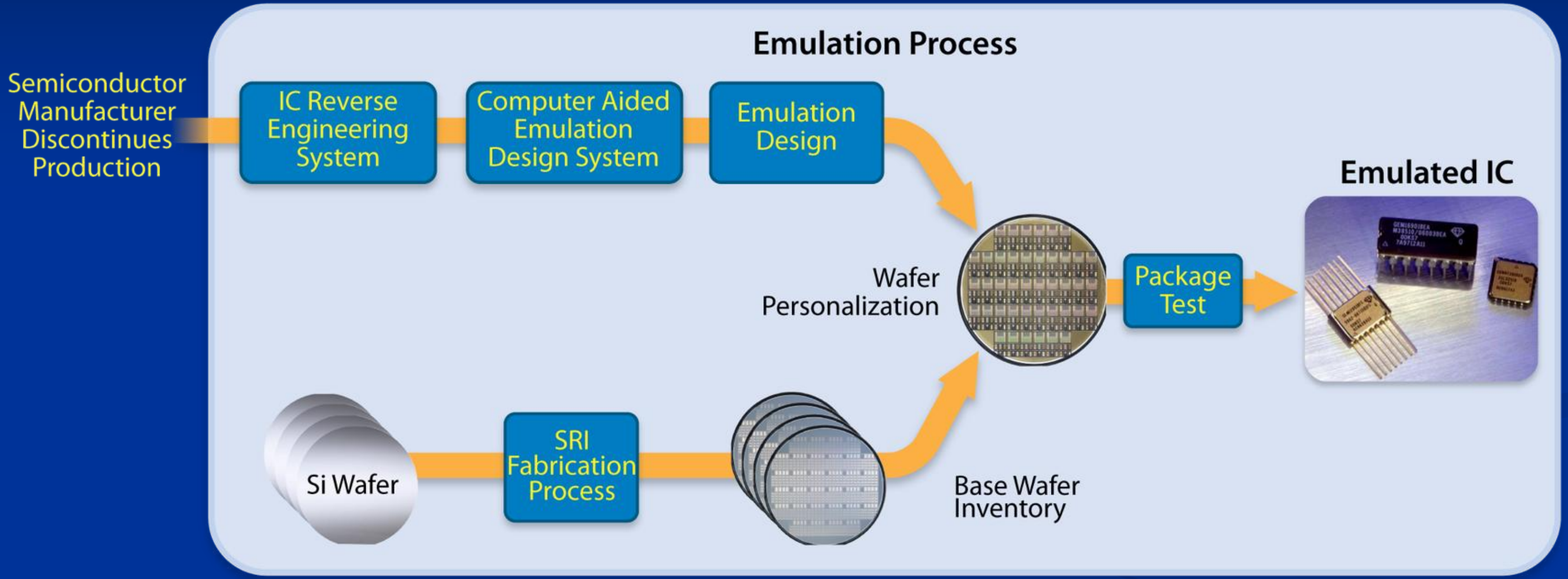
Microcircuit Emulation

… two decades of delivering military quality microcircuits …

- **Emulate ICs ranging from single function complexities to complex ASICs**
  - **Listed on more than 925 military specifications**
  - **Over 100,000 parts delivered**
  - **Stable manufacturing source for over 20,000 part numbers**
  - **Permanent, one-time solution—no end-of-life notice**
- **Over 400 Weapon Systems supported**
  - **Maintain Weapon System readiness**
  - **Avoid MICAP and production shutdowns**
  - **Provide long-term, continuing source for production and sustainment requirements**
- **DoD costs avoidance >$700M**

Microcircuit Emulation Process



- **DLA certified Qualified Manufacturers List (QML) facility**
- **Accredited as a DoD Trusted Foundry supplier to deliver trusted foundry microelectronics**

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B-1B Bomber DMS Problem

- Currently available 54LS193 ICs failed system testing in the Pulse Generator Circuit Card Assembly

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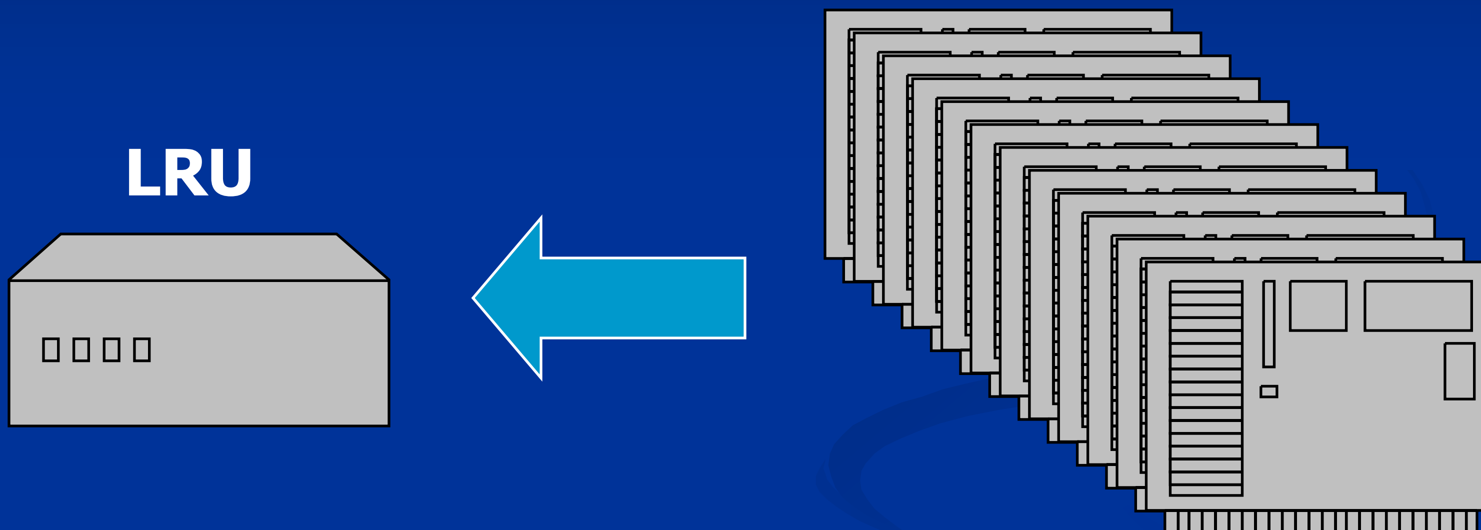
B-1B Bomber Line Replaceable Unit (LRU)



Each CCA board contains eight 54LS193 ICs. The LRU contains twelve CCA boards

Pulse Generator Circuit Card Assembly (CCA)

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54LS193 Manufactured by many Companies

MIL-M-38510/315D

6.8 Manufacturers' designation. Manufacturers' circuits which form a part of this specification are designated with an "X" as shown in table IV herein.

TABLE IV. Manufacturers' designation.

Device type	Circuit	A	B	G	C	E	F	D
	Manufacturer	Texas Instruments, Incorporated	Signetics Corp.	National Semi-Conductor Corp.	Raytheon Company	Fairchild Semi-conductor	Motorola, Inc.	Advanced Micro Devices Inc.
	Commercial Type							
01	54LS90	X	X		X	X	X	
02	54LS93	X	X	X	X	X	X	
03	54LS160A	X	X	X	X	X	X	X
04	54LS161A	X	X	X	X	X	X	X
05	54LS168			X		X		
06	54LS169A			X		X		
07	54LS192	X	X	X	X	X	X	X
08	54LS193	X	X	X	X	X	X	X

Each Company had a Different Specification as Documented by M38510

Parameter	Terminals	Circuits						
		A	B	C	D	E	F	G
		-160/-400	-160/-400	-160/-400	-100/-340	-100/-340	-120/-360	-135/-370
I_{IL9}	A	"	"	"	"	"	"	"
	B	"	"	"	"	"	"	"
	C	"	"	"	"	"	"	"
	D	"	"	"	"	"	"	"
I_{IL10}	Load	-100/-340	"	-150/-380	-120/-360	-120/-360	"	-100/-340
I_{IL11}	Clear	-160/-400	"	-150/-380	"	"	"	-135/-370
	Count up	"	"	"	"	"	"	"
	Count down	"	"	"	"	"	"	"

Only two of the manufactures' parts worked in the system

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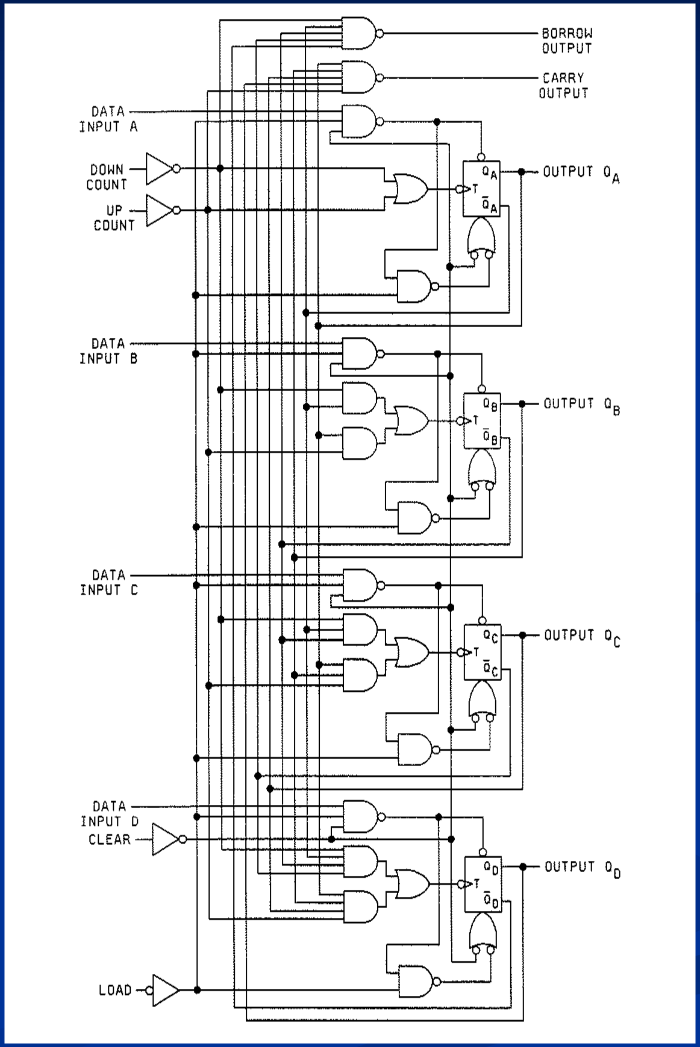
Characterizing the System Requirements

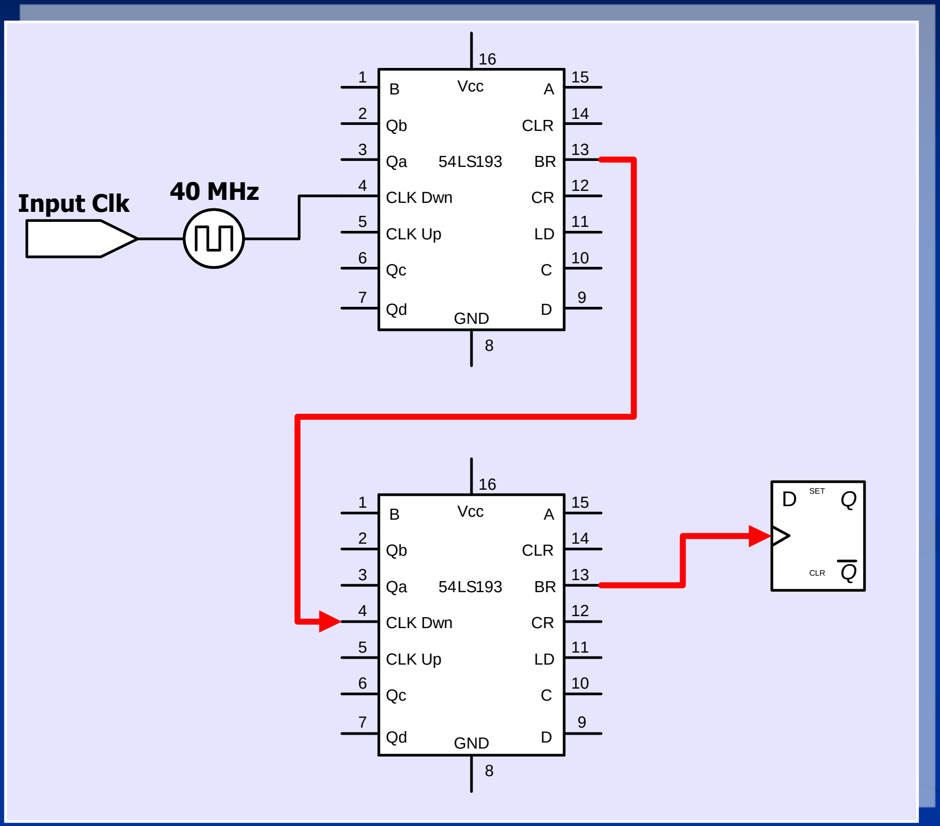
- **The GEM program was used to:**
  - **Evaluate the existing design and components to fully define system requirements**
  - **Design and manufacture QML parts which satisfy the requirements of the application**

54LS193

- **M38510/31508BEA**
- **Synchronous 4-Bit Up-Down Counter with Clear**
- **16-Lead Dual-In-Line Package**



B1-B Pulse Generator 54LS193 Usage



- Borrow output clocks downstream logic
- Carry output has similar logic

Pulse Generator CCA System Specification

- System Clock Rate 40MHz
- M38510 Specifies 54LS193 Fmax minimum = 22MHz
- Part is only screened at 22MHz but operated at 40MHz

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Part Evaluation to M38510 Specification

- An IC that works in the system and an IC that fails in the system were tested to M38510 specifications
- Both ICs passed all parameters over Mil temperature
- Need to look for differences beyond the M38510 parameters

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Bench Testing

- **Fmax**
  - **Both ICs were run at 22MHz and the outputs looked at on a scope**
  - **All outputs from both ICs were clean and functioning properly**
- **System Frequency**
  - **Both ICs were run at 40MHz and all outputs monitored with a scope**
  - **The functional differences between the ICs became apparent at 40MHz operation and the mystery was solved!**

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Part Differences

- The IC that failed system test developed a glitch on the Carry and Borrow output when operated at 40MHz
- The glitch is high enough to double clock downstream logic
- The system schematic shows the carry and borrow outputs are used as clocks for downstream logic

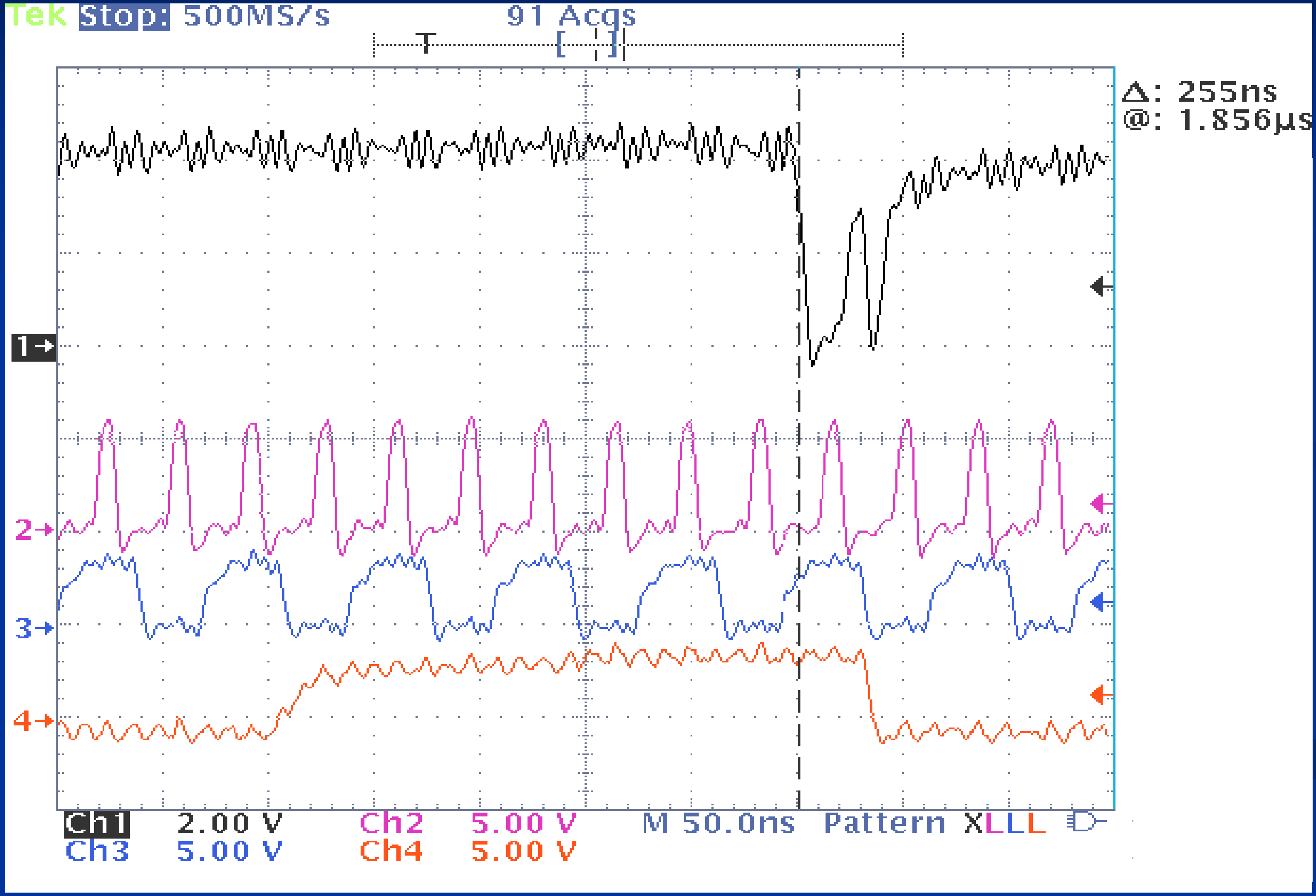
Failed IC Glitch

Carry Output

Up Clk

Qa Output

Qd Output



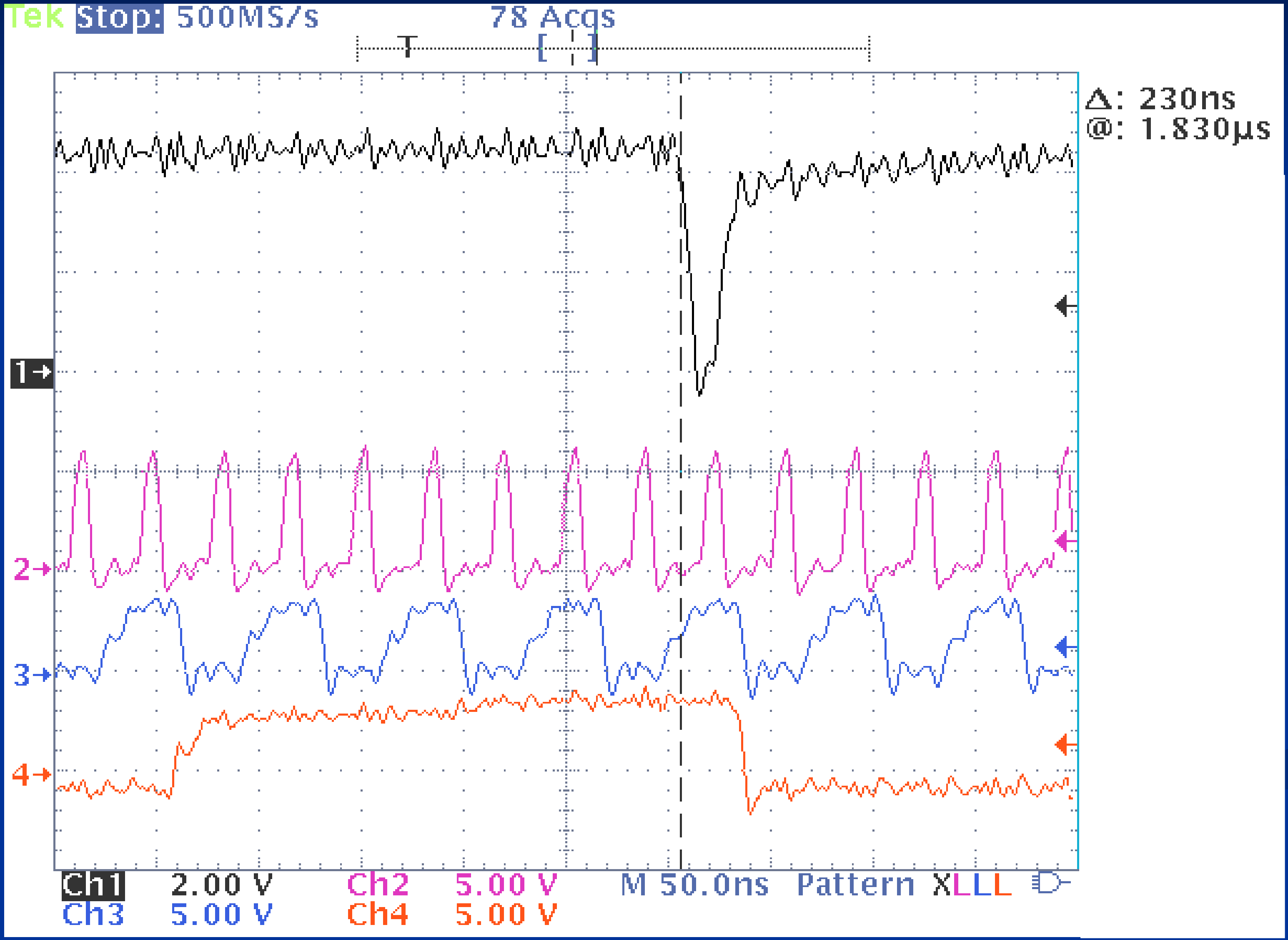
Correct Operation

Carry Output

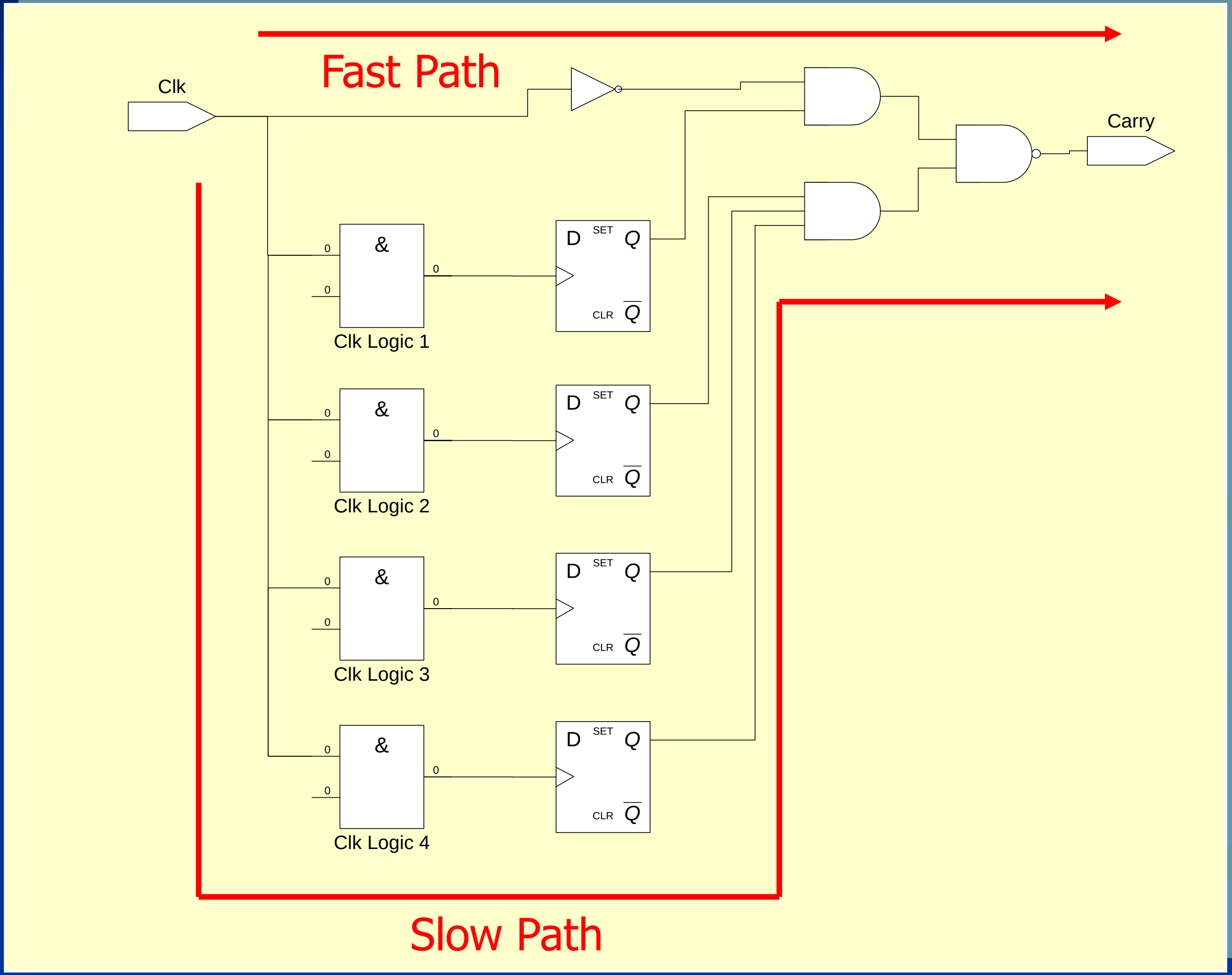
Up Clk

Qa Output

Qd Output

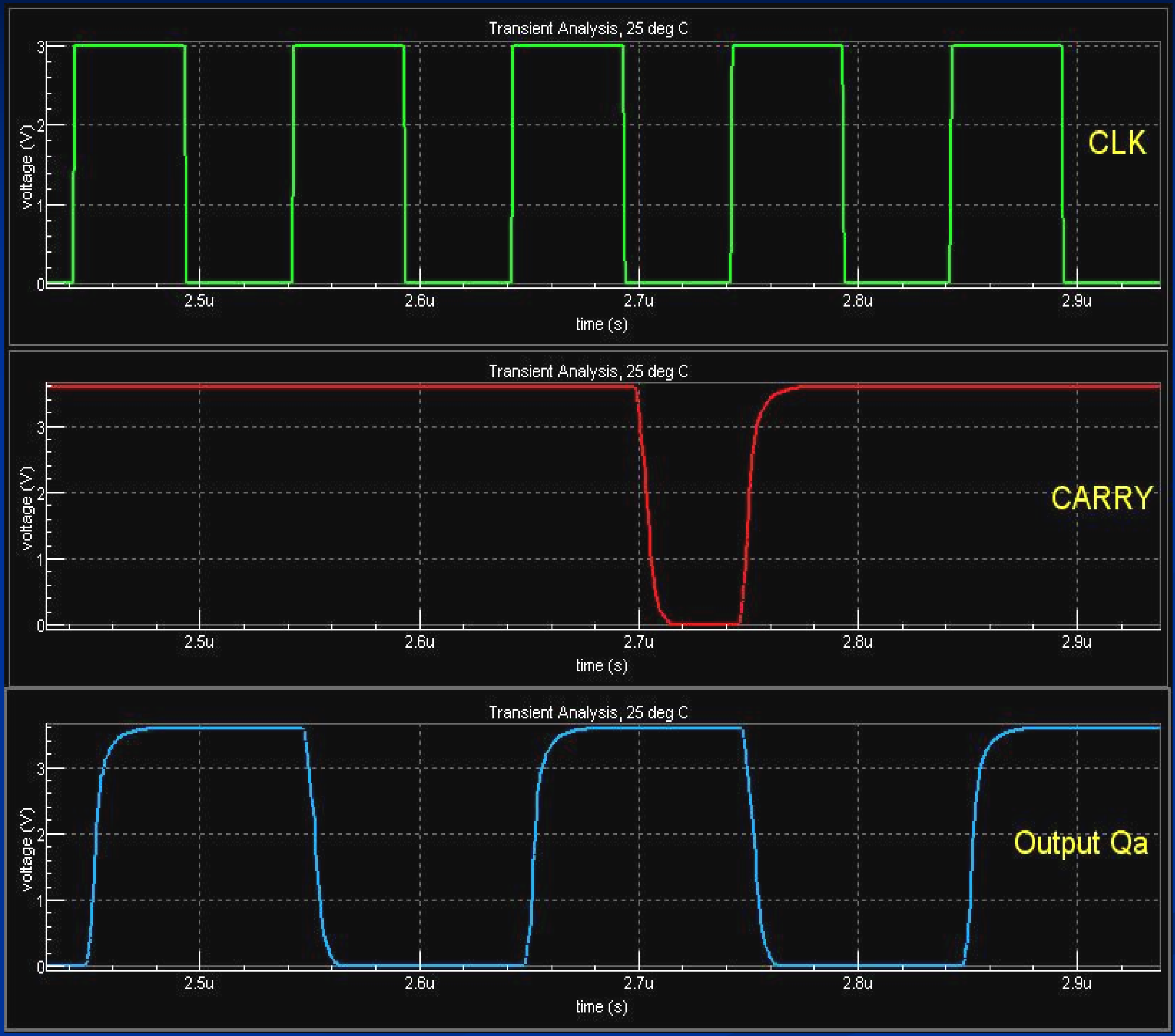


Unbalanced Clock Path Creates Glitch



54LS193 Carry Function

- Q outputs change on rising edge of Clk
- Carry output held high when Clk is high which allows time for Q outputs to propagate to Carry logic
- When Clk goes low, Carry output released



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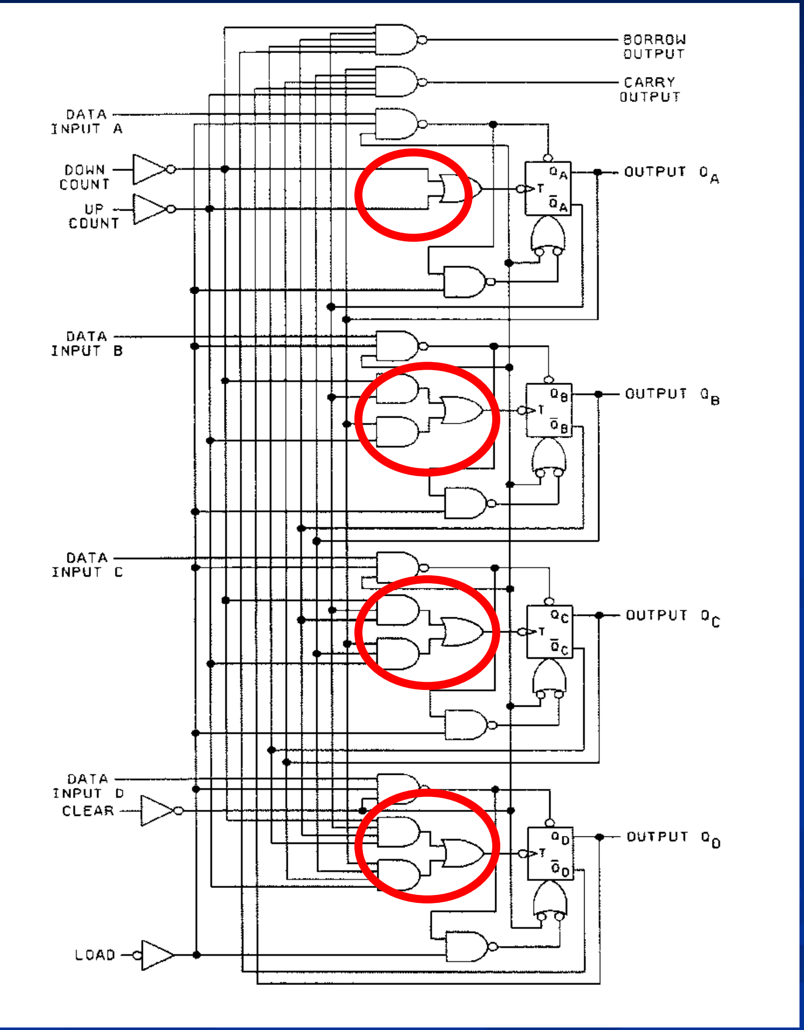
Glitch Cause

- Clock high width cannot be shorter than Q output delay or glitch will occur
- Delay imbalance limits Fmax
- Clock to Carry/Borrow delay needs to be balanced with Q output delay

Original Design

- Every stage has different clock logic
- Clock to Carry/Borrow fastest path
- Clock Fmax limited by Q output delay



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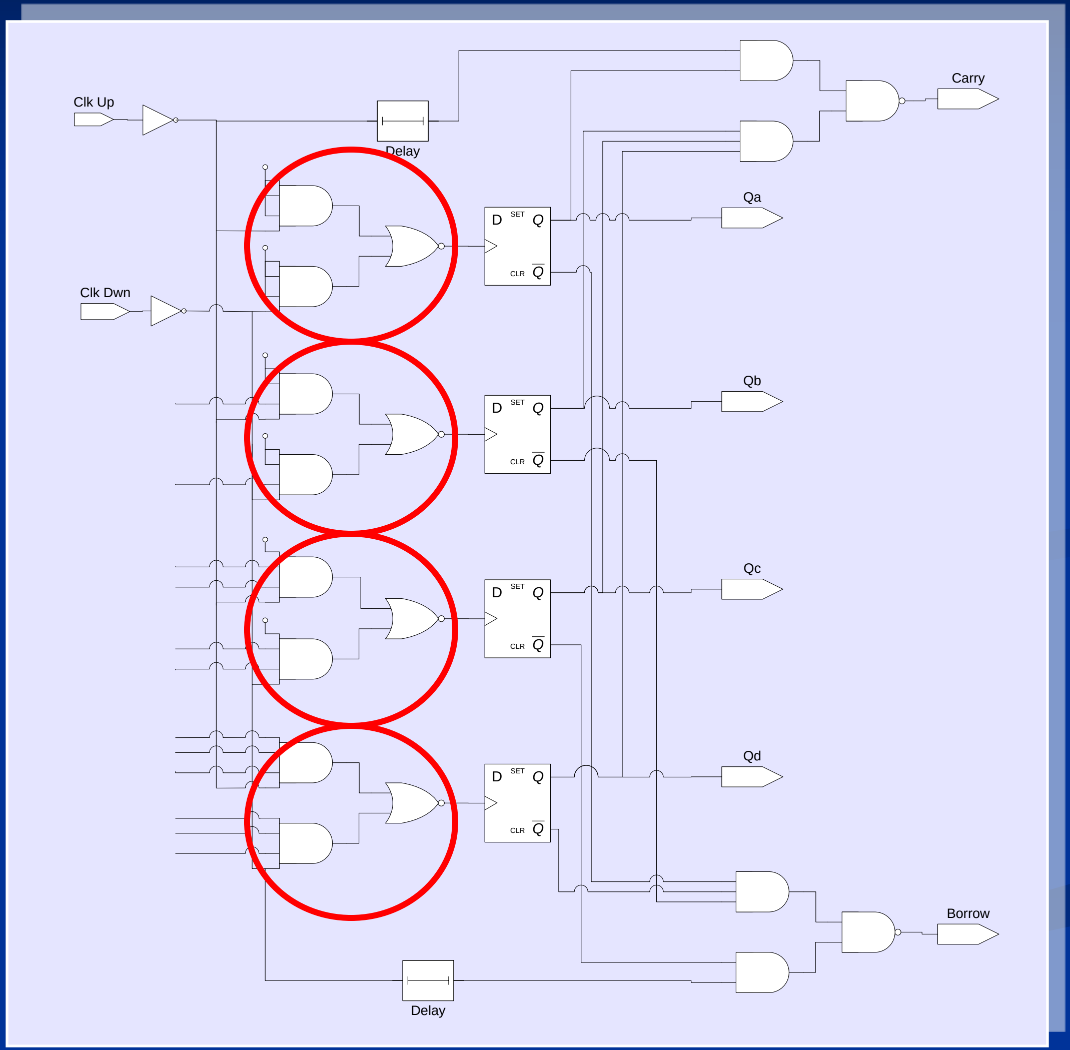
GEM IC Design

- Same logic in each clock path creates balanced Q output delays

- Clk delay blocks adjusted to allow 40MHz glitch-free operation



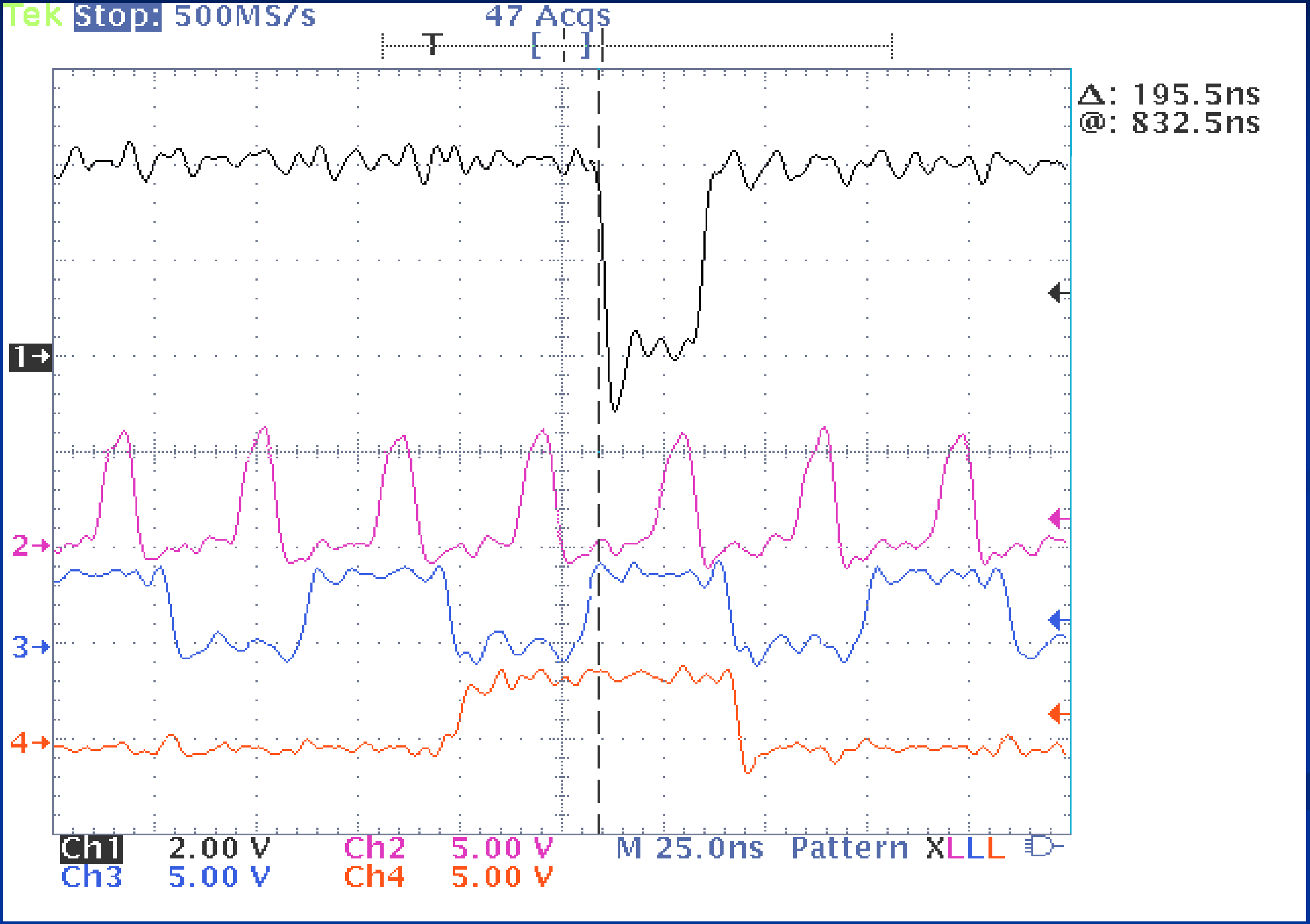
GEM IC Performance

Carry Output

Up Clk

Qa Output

Qd Output



Glitch-free operation - passed all M38510 specifications

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New SMD

- GEM program developed new characterization tests to verify glitch-free operation
- New parameters measure the difference between the Clock to Carry/Borrow and Clock to Q delays and set a limit so at 40MHz operation, a glitch will not develop
- New SMD created to include additional performance requirements not specified by the existing mil spec

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Conclusion

- GEM Program reverse engineered part failure problem in B1-B Bomber LRU
- GEM designed and manufactured QML ICs which satisfy the requirements of the application
- New SMD was created which includes additional parameters to assure 40MHz glitch-free operation and allows procurement
- Systems that rely on unspecified IC characteristics can introduce future DMS problems
- GEM program uniquely qualified to solve DMS problems by having reverse engineering, design, test and fab under one roof

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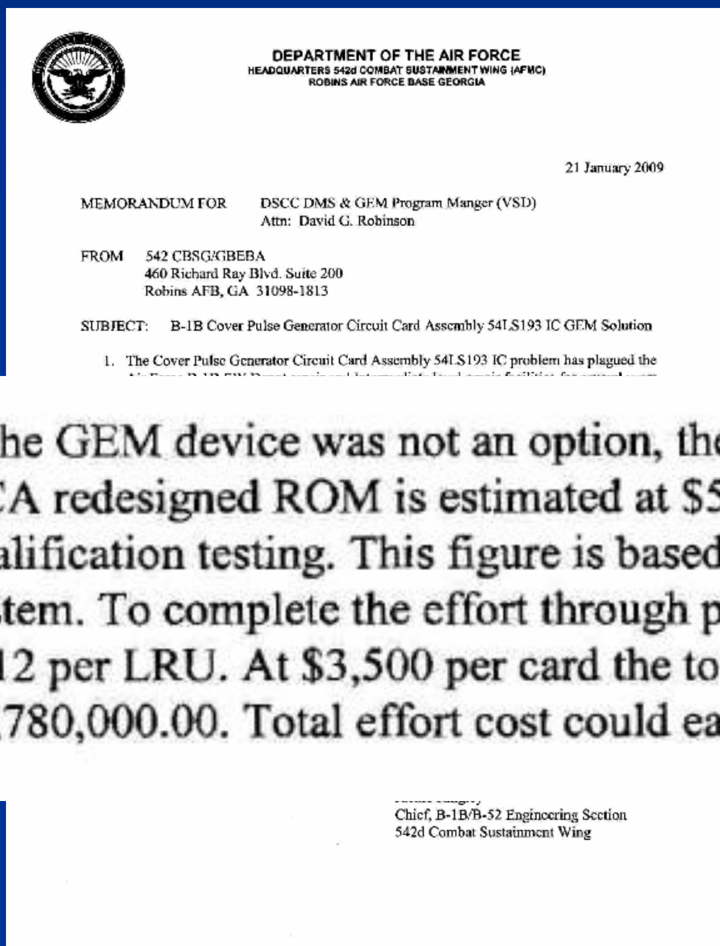
Conclusion



DEPARTMENT OF THE AIR FORCE
HEADQUARTERS 542d COMBAT SUSTAINMENT WING (AFMC)
ROBINS AIR FORCE BASE GEORGIA

21 January 2009

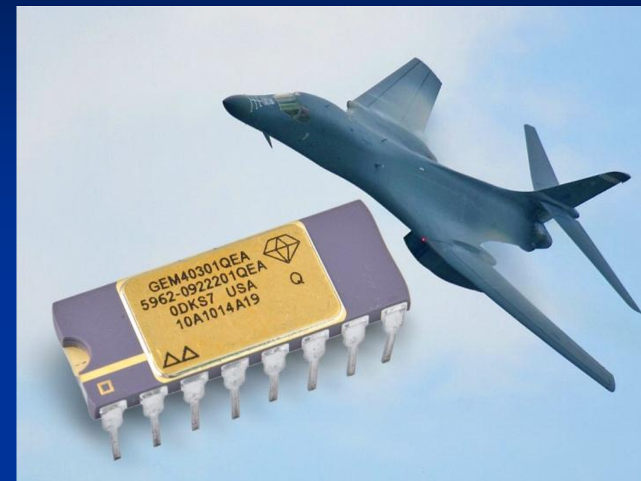
MEMORANDUM FOR DSCC DMS & GEM Program Manger (VSD)
Attn: David G. Robinson

FROM 542 CBSG/GBEBA
460 Richard Ray Blvd. Suite 200
Robins AFB, GA 31098-1813

SUBJECT: B-1B Cover Pulse Generator Circuit Card Assembly 54LS193 IC GEM Solution

1. The Cover Pulse Generator Circuit Card Assembly 54LS193 IC problem has plagued the

Chief, B-1B/B-52 Engineering Section
542d Combat Sustainment Wing



If the GEM device was not an option, the circuit card would have to be redesigned. A CCA redesigned ROM is estimated at $500,000.00 to carry project through redesign and qualification testing. This figure is based upon similar efforts on the ALQ-161 defensive system. To complete the effort through production would require new CCAs for 90 LRU at 12 per LRU. At $3,500 per card the total production cost would run an estimated $3,780,000.00. Total effort cost could easily top $4,280,000.00.

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