Wafer Level Packaging for High-Aspect Ratio MEMS

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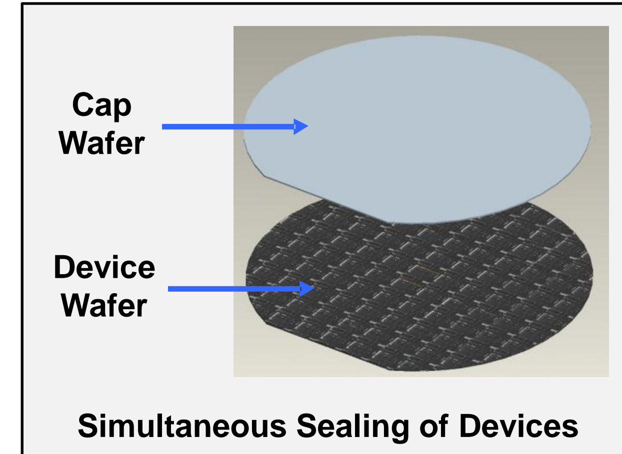
Project Description

- Joint Fuze Technology Program (JFTP) sponsored project
- Objective
  - Develop wafer level packaging techniques that are applicable to high-aspect ratio MEMS devices
    - Wafer bonding for hermetic package sealing
    - Through vias for electrical connection to sealed devices
- Impact
  - Improved reliability and safety of MEMS components
    - S&A chip
    - Rocket motor igniters
    - Environmental sensors
  - Increased throughput and yield of the MEMS manufacturing process
  - Lower cost components



Simultaneous Sealing of Devices

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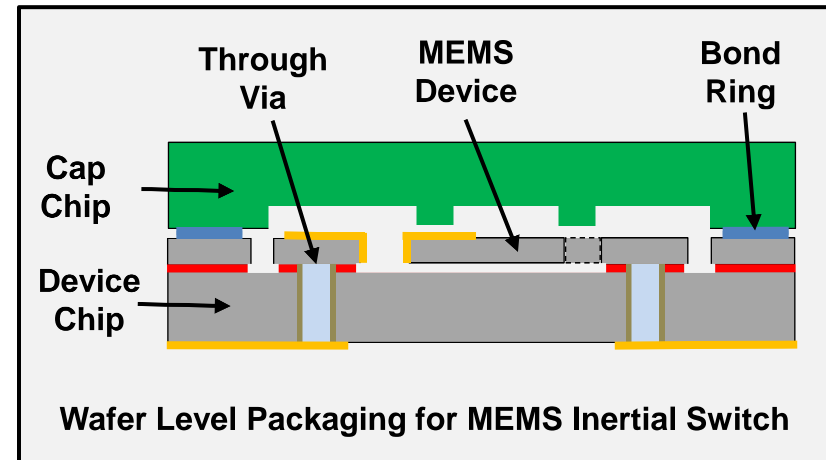
MEMS Package Requirements

- Compatible with existing device designs and fabrication sequence
- Bond strength
  - Survive g-loading up to 50 Kg's
  - Die shear strength > 15 MPa
- Hermeticity
  - > 10 year storage
  - Leak rate < 10^{-11} atm-cc/sec
- Provide electrical path to interior of sealed package
- Devices to be packaged
  - Current focus is on inertial switches
  - Extension to packages with energetic materials
    - Wafer bonding after energetic materials are deposited
    - Requires low temperature bonding or localized heating



Wafer Level Packaging for MEMS Inertial Switch

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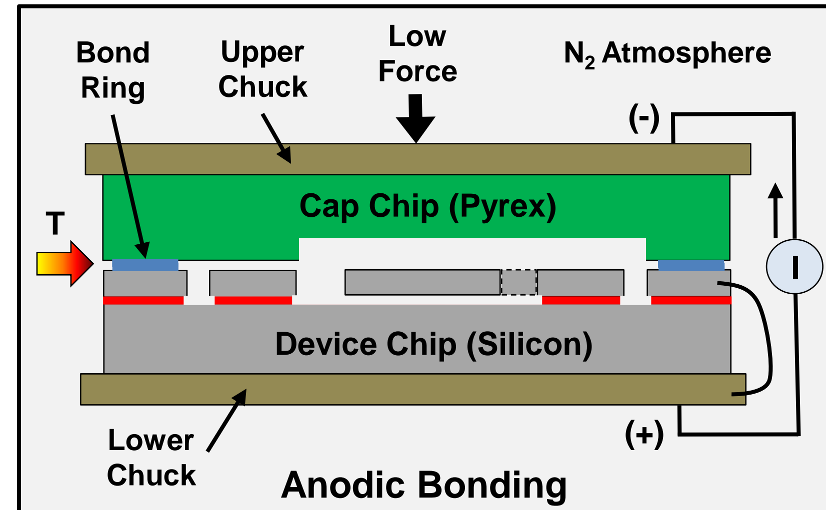
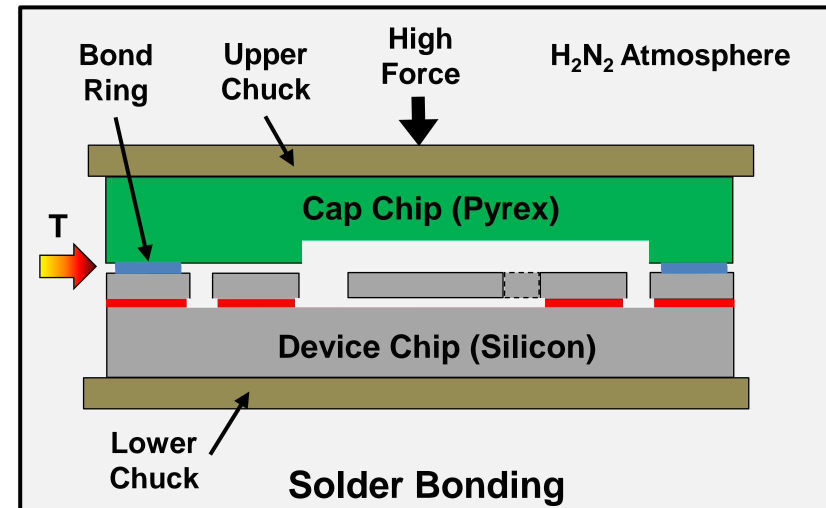
Background: Wafer Bonding

- A device and cap wafer are precisely aligned and bonded under temperature and pressure in a controlled atmosphere
- Allows the simultaneous sealing of 100s to 1,000s of MEMS devices
- Wafer bonding techniques
  - Anodic: silicon to glass bonding with a large applied electric field
  - Solder: intermediate solder layer bonds metallic pads on each wafer
  - Eutectic: bonding with an intermediate material that forms a eutectic alloy with silicon
  - Fusion: direct silicon to silicon bonding





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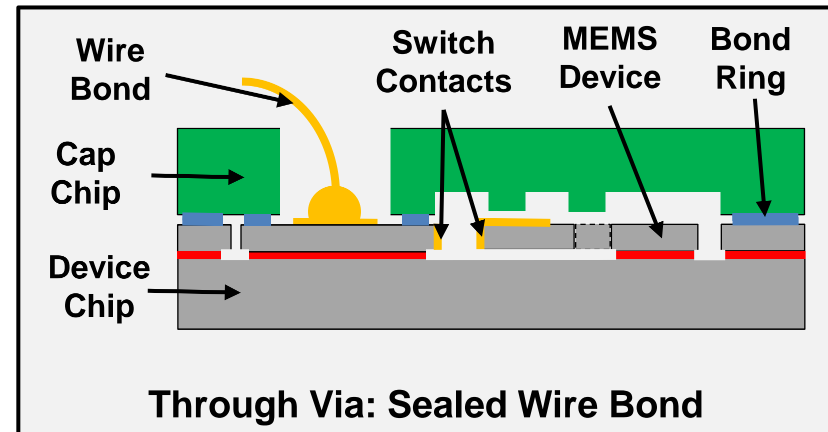
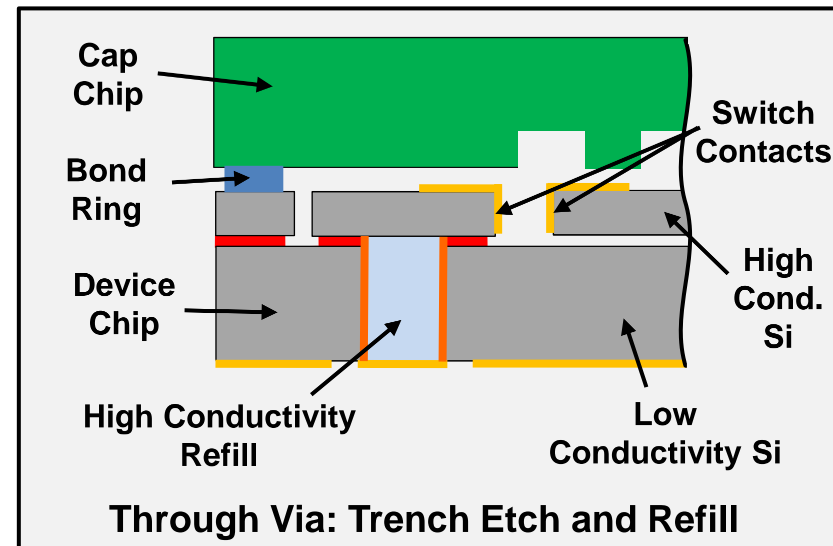
Background: Through Vias

- Provide an electrical path to the MEMS devices while maintaining environmental isolation
- Through via techniques
  - Sealed wire bonds
  - Trench etch / refill
    - Trench is etched through the wafer
    - Can be coated with a dielectric material (SiO_2 or nitride)
    - Refill with a conductive material
      - Metal
        - Electroplating
        - Conductive paste
      - Polysilicon
  - Buried traces under bond ring



Through Via: Sealed Wire Bond



Through Via: Trench Etch and Refill

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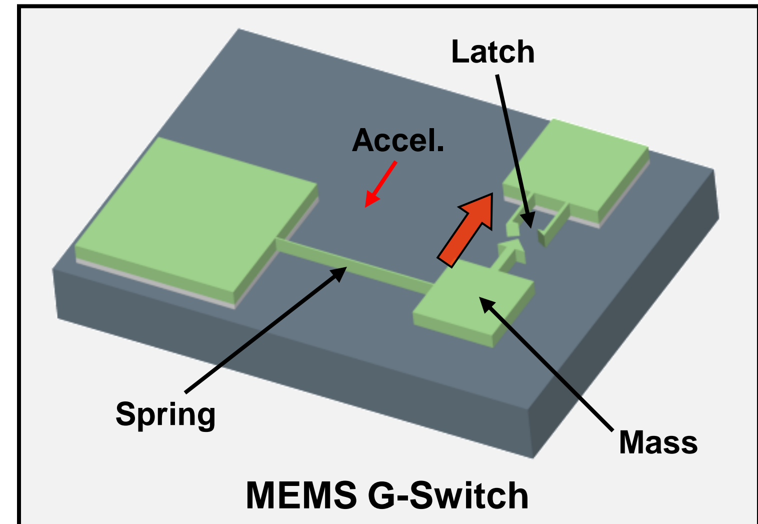
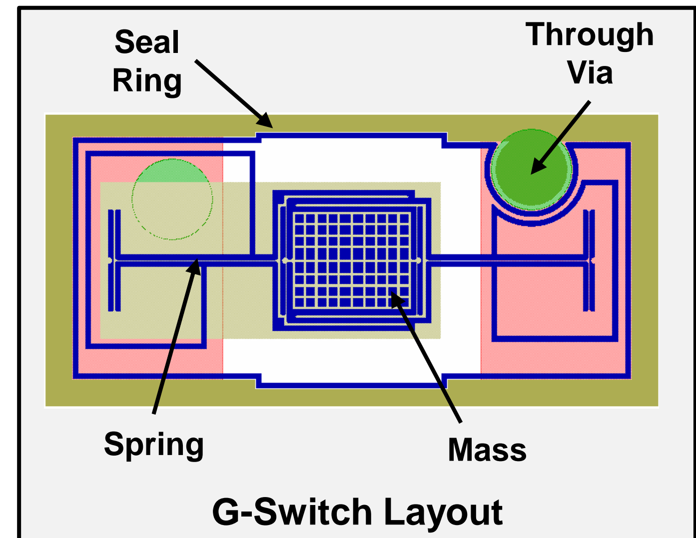
MEMS Device Design

- **G-Switch**
  - Spring supported mass that displaces under acceleration
  - Retard Sensor
    - Design activation level: 1.5 - 5 g's
    - Unidirectional motion
  - Impact Sensor
    - Design activation level: 60 - 120 g's
    - Unidirectional or multidirectional motion
- **Restrict out-of-plane motion without inducing stiction during bonding**
- **Devices designed in conjunction with JFTP project "MEMS Retard and Impact Sensors"**



MEMS G-Switch



G-Switch Layout

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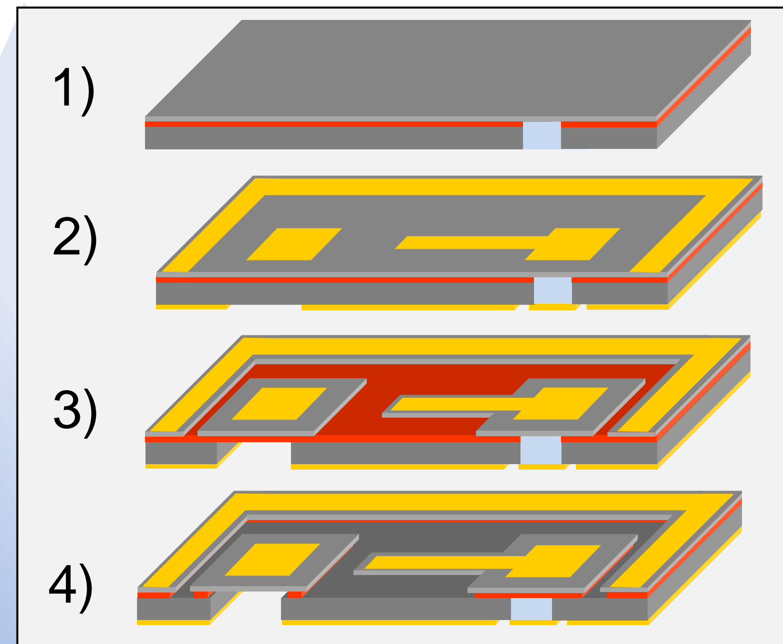
Fabrication: Solder Bonding

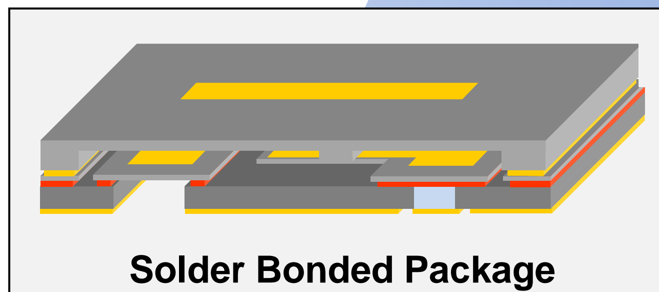
- **Device wafer fabrication**
  - Deep reactive ion etching (DRIE) based sequence
  - Silicon on Insulator (SOI) substrate

1. Through via formation
2. Frontside / backside metallization
3. Frontside / backside DRIE
4. Vapor HF release

- **Cap wafer fabrication**
  - Silicon or glass substrate

1. Frontside metallization (AuSn solder) Backside metallization
2. Frontside etch





Solder Bonded Package

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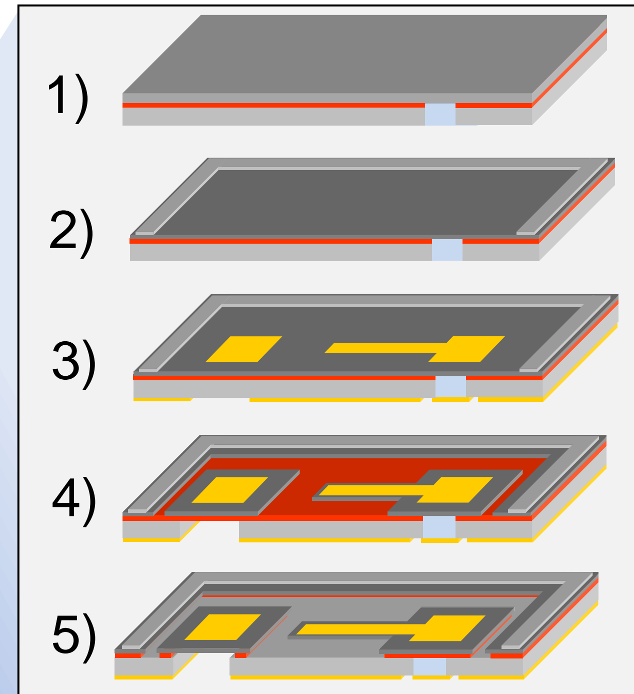
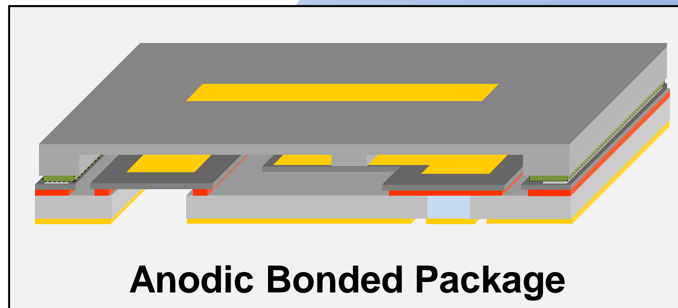
Fabrication: Anodic Bonding

- **Device wafer fabrication**
  - **Deep reactive ion etching (DRIE) based sequence**
  - **SOI substrate**
  1. **Through via formation**
  2. **Frontside DRIE**
  3. **Frontside / backside metallization**
  4. **Frontside / backside DRIE**
  5. **Vapor HF release**
- **Cap wafer fabrication**
  - **Silicon or glass substrate**
  1. **Backside metallization**
  2. **Frontside glass deposition (silicon substrate only)**
  3. **Frontside etch**





Anodic Bonded Package

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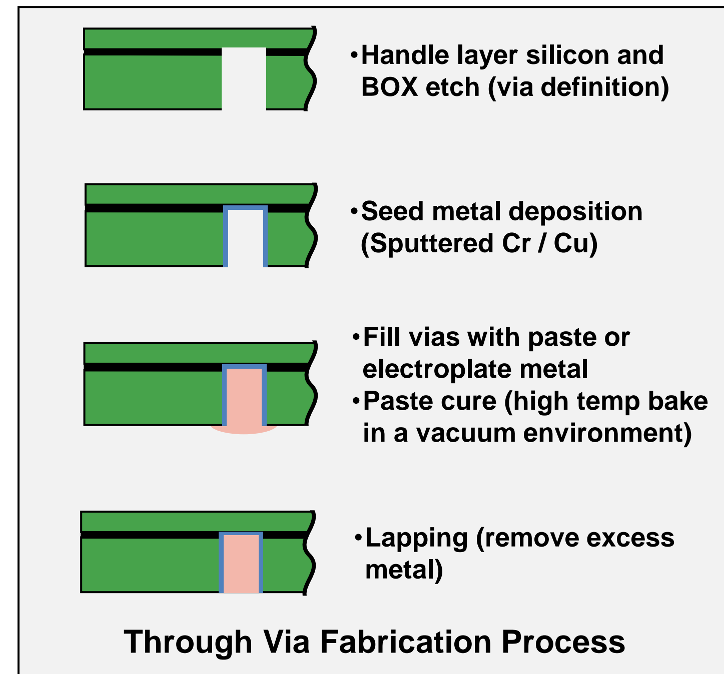
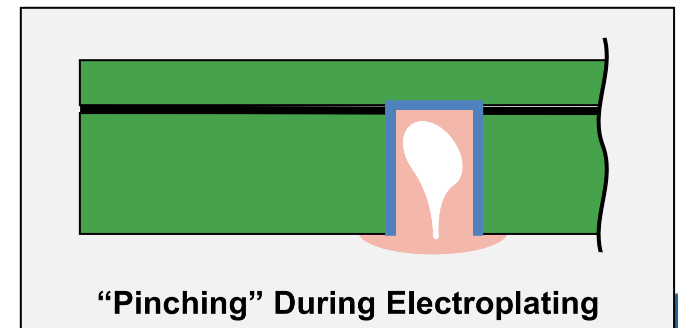
Fabrication: Through Vias

- "Via first" approach
  - Vias are created at the beginning of the process flow
  - MEMS devices created later in the process flow
- DRIE through handle layer to create vias that connect to backside of device layer
  - Vias isolated by high resistivity handle silicon and device layer trenches
- Fill vias with metal
  - Conductive paste (short-term solution)
    - Requires bake
    - Susceptible to voids
  - Electroplating (long-term solution)
    - High aspect ratio vias cause the metal to "pinch" at the top of the via
    - JHUAPL is developing process to eliminate pinching



Through Via Fabrication Process


"Pinching" During Electroplating

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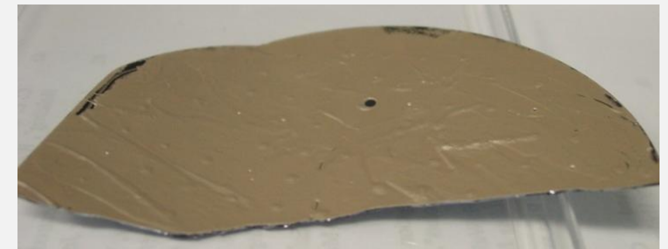
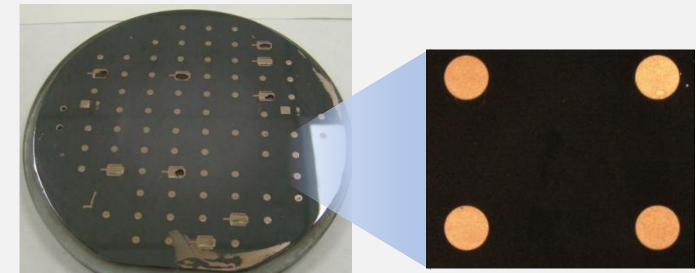
Fabricated Through Vias

- **Via metal fill**
  - Conductive paste (Ag coated Cu powder)
  - Via fill cured with high temp. bake in a vacuum environment
  - Lapping to remove overfill
- **Initial wafer problems**
  - Single paste fill and bake steps
  - Caused voids in vias and wafer warpage
  - Solved by performing multiple paste fill and bake steps
- **Electrical resistance**
  - Measured < 1 Ohm from top of via to top of device layer silicon



Warped wafer due to paste shrinkage during cure

Filled vias post-cure before lapping



Completed wafer with lapped vias

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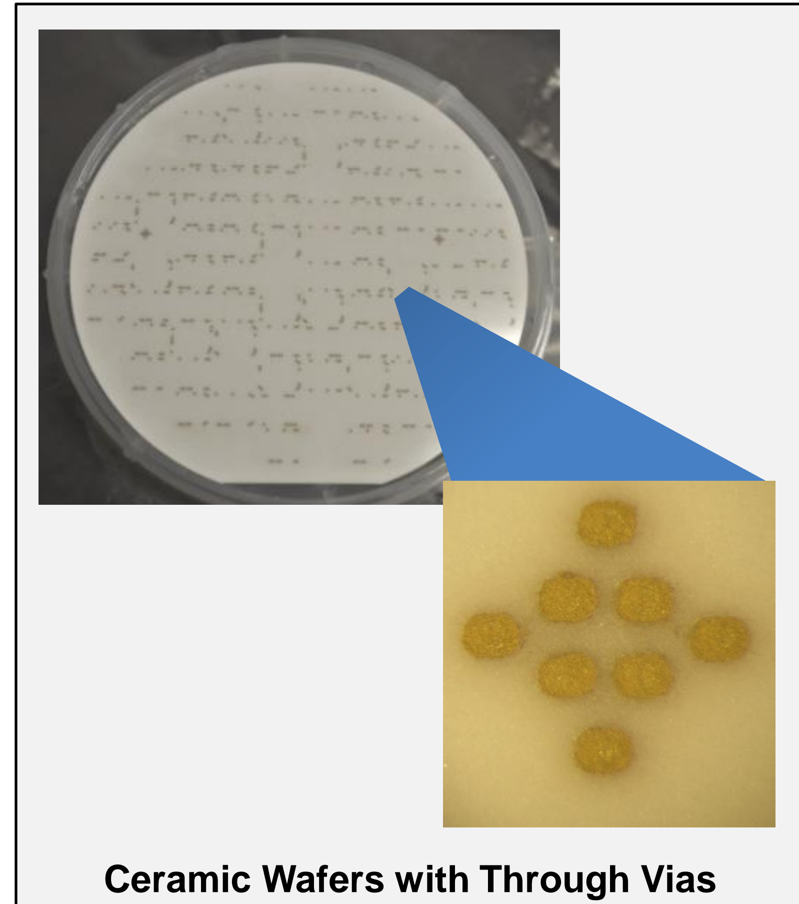
Commercial Through Vias

- **Baseline to compare in-house designs**
- **Wafer description**
  - **Ceramic wafers with laser drilled through vias**
  - **Vias filled with Au particles suspended in thinner**
  - **Via fill cured with high temp. bake**
- **Electrical resistance**
  - **Measured .1 Ohm from frontside to backside of via**
- **AuSn solder deposited for bonding with device wafer**



Ceramic Wafers with Through Vias

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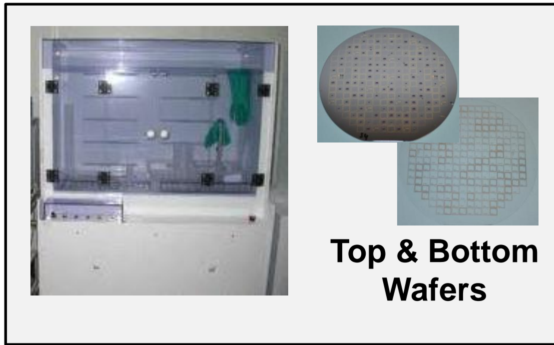
Assembly & Evaluation Process

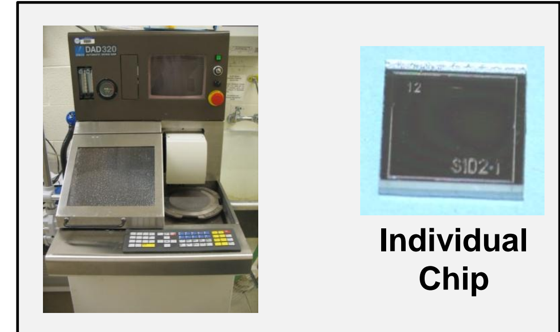
Sealed Chip Assembly

Cleaning → Alignment → Bonding → Dicing →



Top & Bottom Wafers

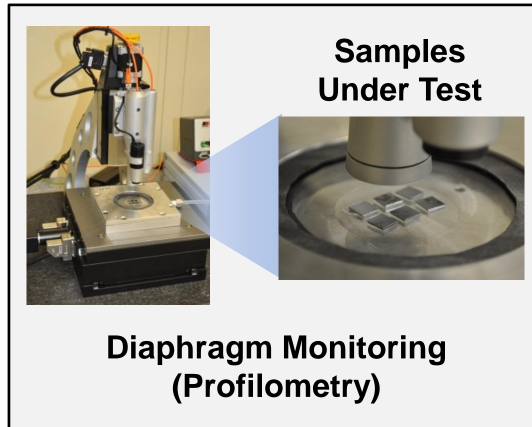
Bonded Pair



Individual Chip

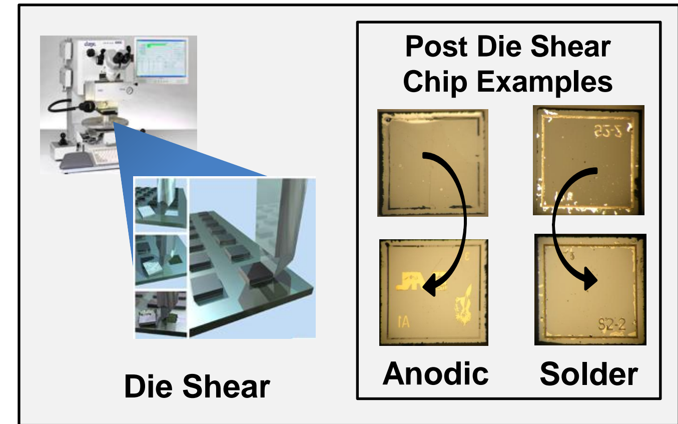
→ Visual Inspection → Hermeticity → Bond Strength

- Dicing water intrusion
- Interference fringes
- Bond ring appearance
  - Anodic: darker in color
  - Solder: squeeze-out
- Bond ring alignment



Samples Under Test

Diaphragm Monitoring (Profilometry)



Die Shear

Post Die Shear Chip Examples

Anodic Solder

Bond Evaluation

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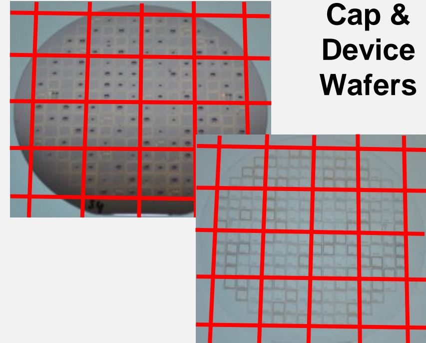
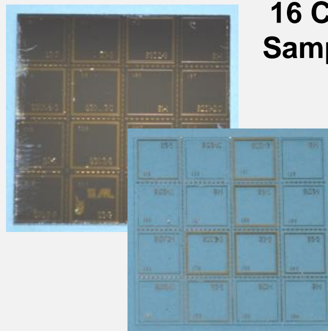
Bonding Process

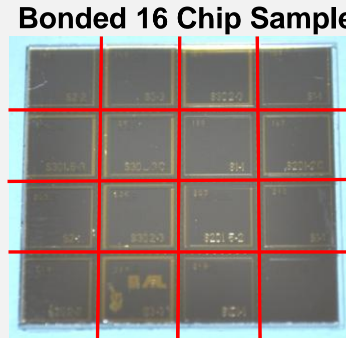


Cap & Device Wafers



16 Chip Samples

Bonded 16 Chip Sample



16 Individual Chips

Dicing → Cleaning → Alignment → Bonding → Dicing → Bond Evaluation

Dicing Saw

Wafer Aligner / Bonder

Bond Parameters

AuSn Solder	Anodic
300-380 °C	320-400 °C
2000-3000 N	<1000 N
650-760 Torr	650-760 Torr
H_2N_2 Purge	N_2 Purge
30-60 min.	15-30 min.
	400-1000 V

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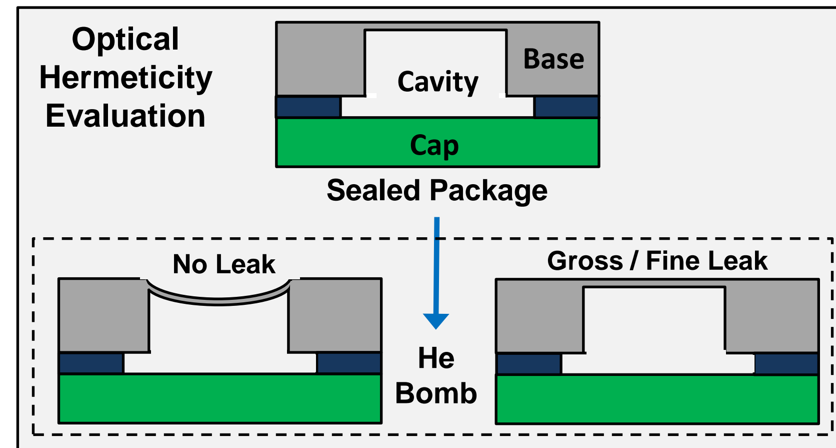
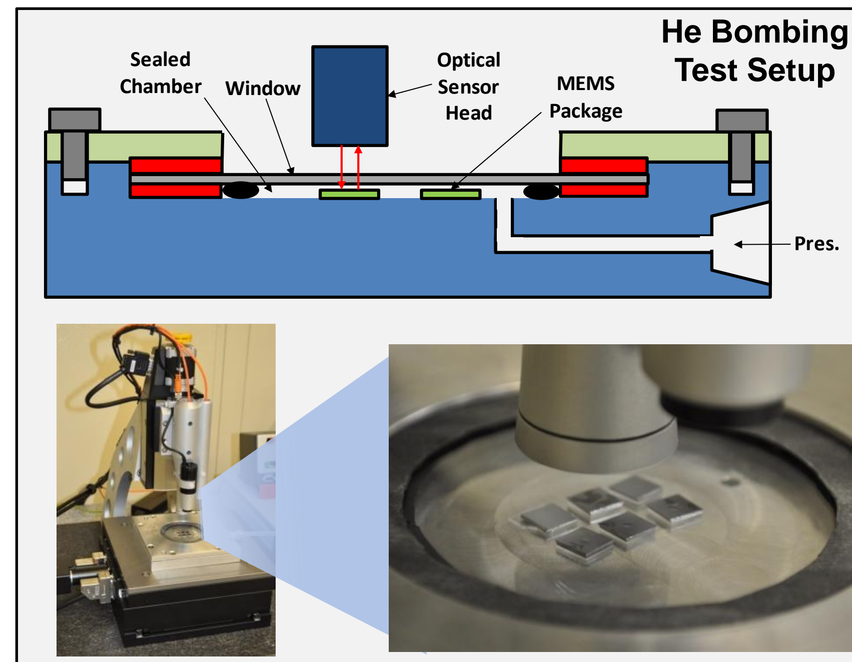
Hermeticity Evaluation

- **Diaphragm deflection observed post-bonding**
- **Optical profilometry**
  - Packages placed in sealed chamber that is pressurized with a gas
  - Diaphragm deflects with pressure differential on either side of cavity
- **Helium (He) utilized to detect leaks more quickly**
  - Actual leak rate in air calculated
  - Min. detectable leak rate:

    10^{-12} - 10^{-13} atm-cc/sec
- **Fixture designed and manufactured**
- **Anodic and solder samples evaluated**
  - Total test time of 40-60 hours
  - Deflections measurements performed every 5-20 hours





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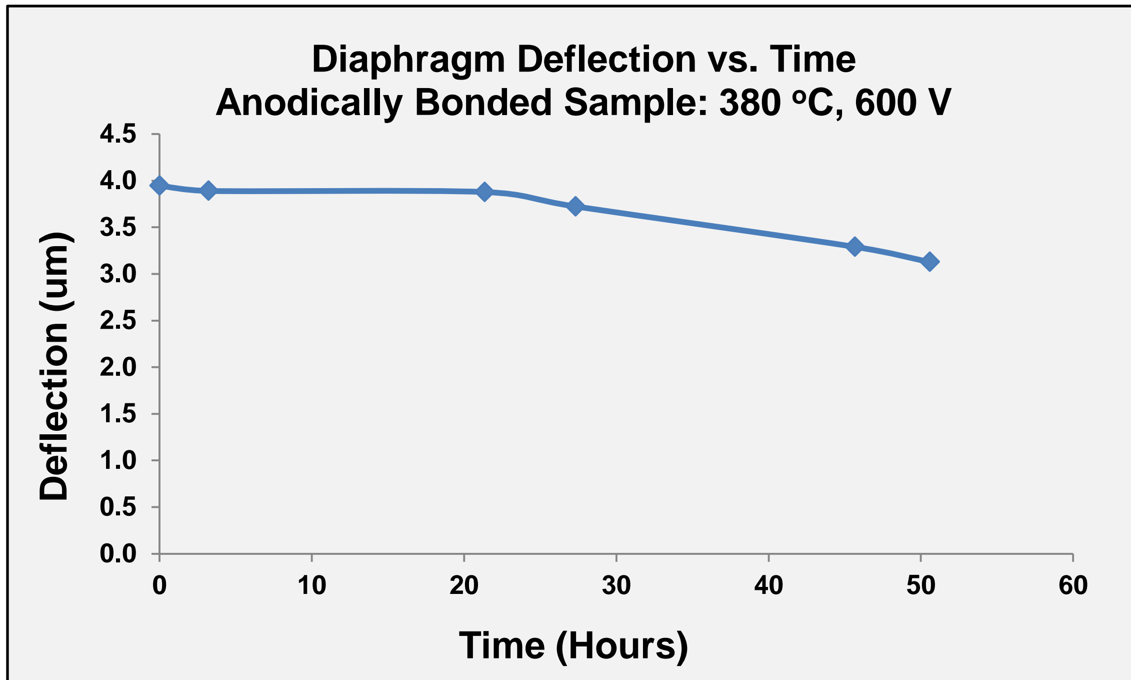
Hermeticity Evaluation



Test Parameters

Package Volume	.0001 cc
He Bomb Pressure	2.93 atm
Package Seal. Pres.	.90 atm

Measured He Leak Rate
4.37E-10 atm-cc/sec

Equivalent Leak Rate in Air (Standard Leak Rate)
1.63E-10 atm-cc/sec

- **General correlation with bond parameters**
  - **Higher temperature, bond pressure, voltage results in samples with better hermetic seal**
- **Chips from a bonded sample will all generally exhibit a good bond (acceptable leak rate) or all exhibit gross leaks / no seal**

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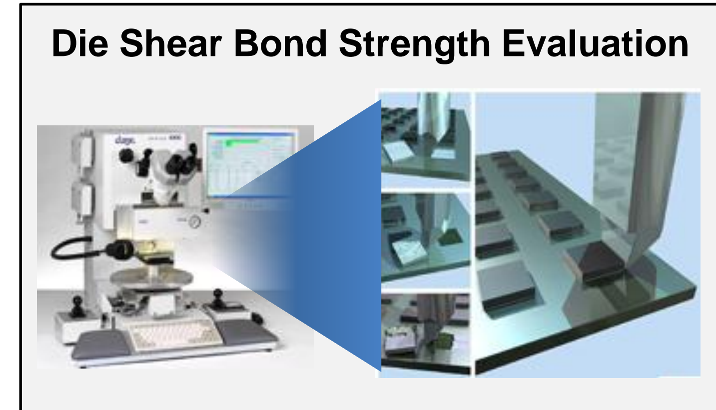
Bond Strength Evaluation

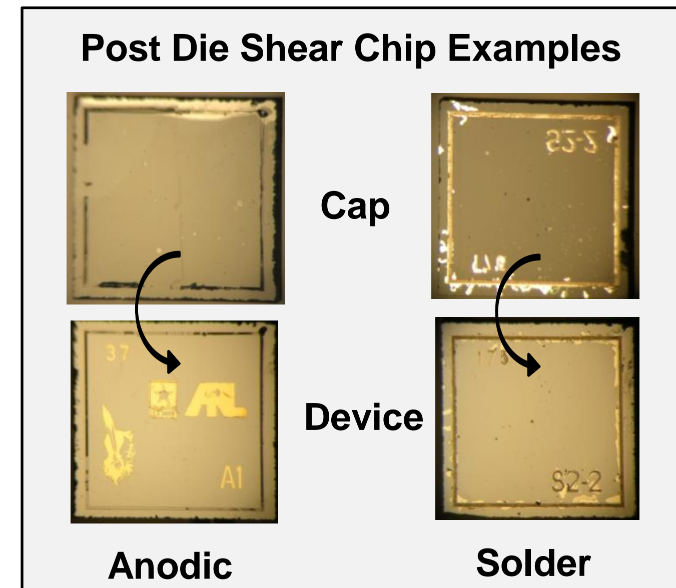
- Visual inspection indicates uniform bonds
  - Dark anodic bond lines
  - Solder squeeze out from bond lines
  - Concentric interference fringes
- Some bond inconsistencies observed in completed packages
  - Due to non-uniform pressure application and chip contamination
- Die shear evaluation
  - Stress induced parallel to the plane of the bond until failure occurs

Method	Average Bond Strength	Bond Characteristics	Ideal Bond Parameters
Anodic	35 MPa	• Chips fracture before bond • Material transfer between chips	350 °C 400 V
Solder	28 MPa	• AuSn solder transfer to device chip bond areas	320 °C 3000 N

Die Shear Bond Strength Evaluation



Post Die Shear Chip Examples



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Project Summary

- Developing wafer level packaging techniques that are applicable to high-aspect ratio MEMS devices
  - AuSn solder and anodic bonding for hermetic package sealing
  - Electrical through vias for electrical connection to sealed devices
- Packaging of a MEMS inertial switch for retard and impact sensing
- Successfully assembled packages with required bond strength and hermeticity
- Developed technique for through via formation
- Next step: fully evaluate bonded inertial sensor performance
- The completed work will:
  - Improve the manufacturability and reliability of MEMS components in the fuze, including sensors and/or the MEMS S&A chip
  - Lead to higher process throughput and lower cost components

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