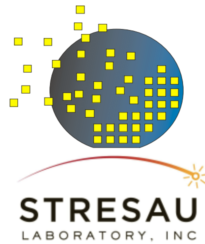
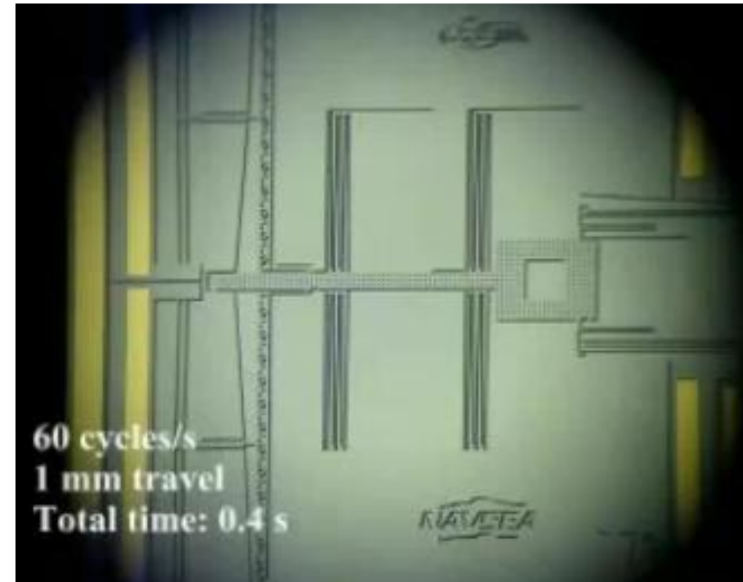
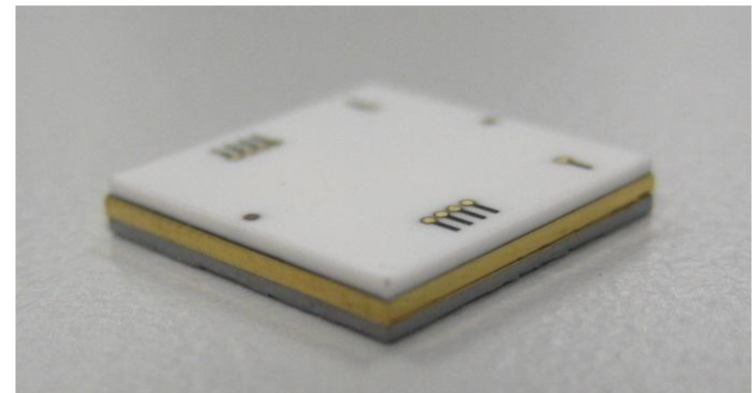
MEMS Fuze-on-a-Chip

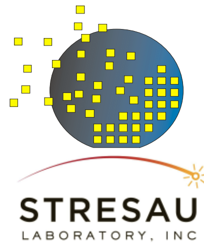


- Low-Cost Fuzes
- Scalable
  Production Process
- Enormous Silicon
  Manufacturing
  Infrastructure





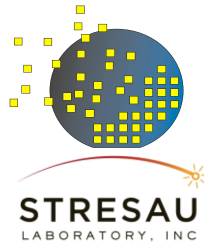
Team



- Navy: Design, Prototype, Pilot Production
- Army: Explosive Train
- MicroAssembly/Laserlith: FEA, Packaging and Integration, Production
- Stresau Laboratory: Loading, Testing

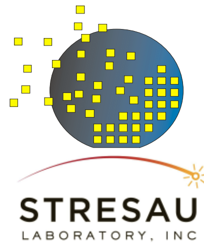
- Progress
  - Low-Temperature Wafer Scale Packaging
  - Fabrication Iterations of Navy S&A Design
  - High-G Results of Navy S&A Design

MicroAssembly



- Operating since 1998
- Partnership
  - Navy S&A Design
  - Army EDF-11 Integration
  - Room-Temperature Hermetic Sealing Process Compatible with Energetic Materials
- Technology Transition
  - New MEMS Manufacturing Cleanroom
  - Loading and Packaging Facility for Volume Production

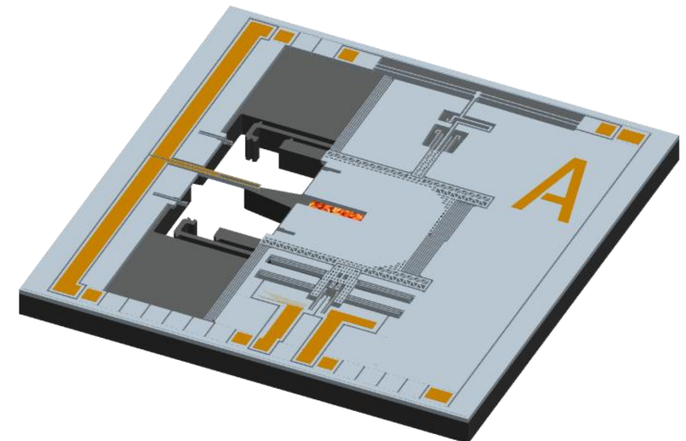
Outline



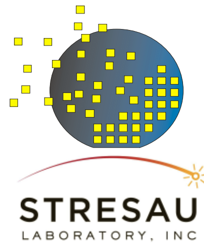
- Fabrication of Navy S&A Design
- Packaging
- Cost and Capacity
- Manufacturing
- Next Steps

Fuze Approaches

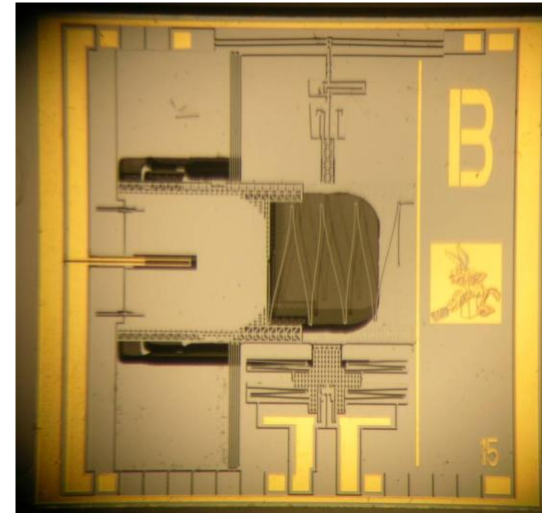
Approach	Safe & Arm	Hermetic Packaging for Long Shelf Life
Traditional	Watchmaker	One at a Time
Navy/MicroAssembly	COTS Silicon DRIE	Batch
Other Approaches	LIGA Multilayer Metal	One at a Time

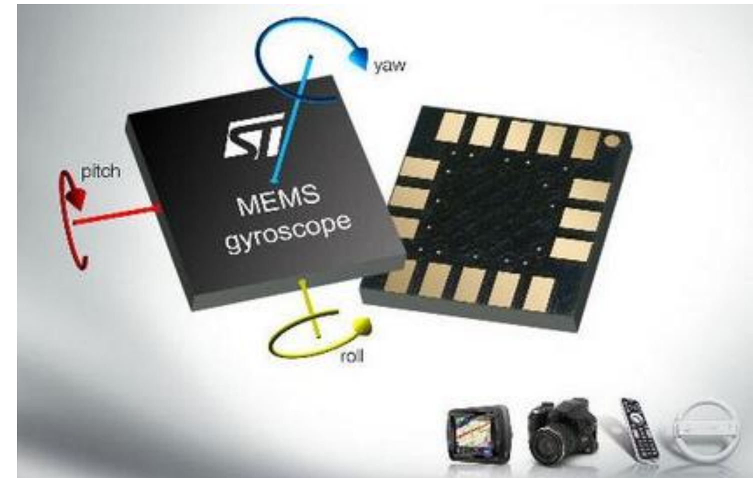


COTS Silicon Safe & Arm

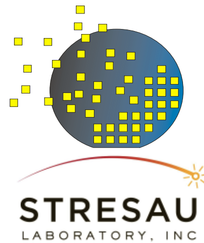


- Navy Design << $30
  - Enabler: COTS Deep Reactive Ion Etcher (DRIE)
  - Driver: MEMS Gyroscopes
- Industry Base
  - At Least 1 COTS DRIE Etcher per Foundry
  - Team Owns 2 Etchers
- MEMS Gyroscopes
  - Millions of Units per Year
  - Cell phones, Automotive Stability
  - InvenSense, Seiko Epson, STMicroelectronics, Analog Devices

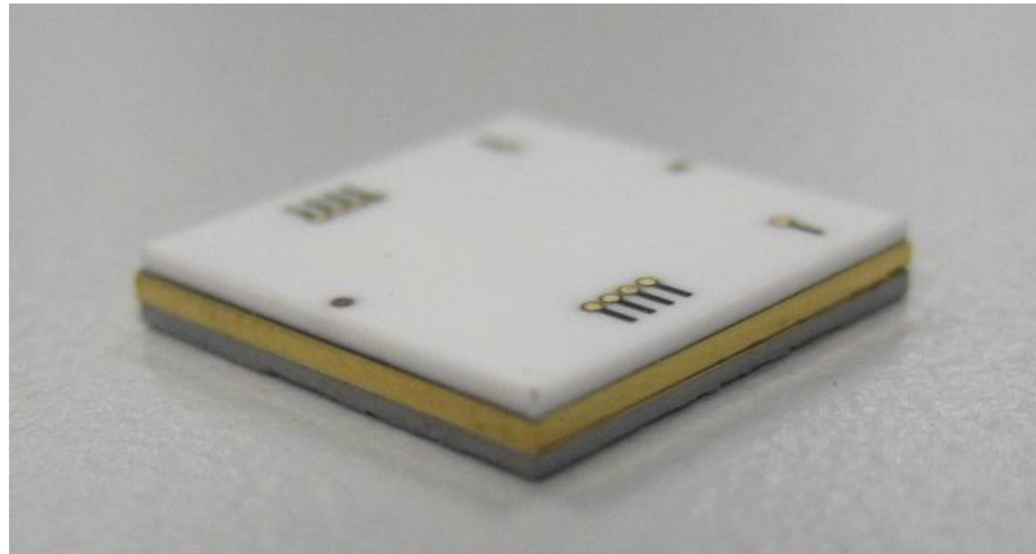




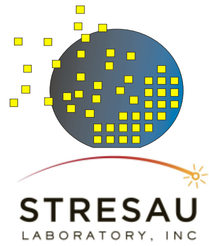
Key Milestone



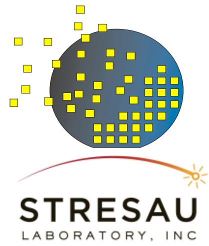
- Hermetically Packaged MEMS S&A With Scalable Packaging Process



3 Chip Architecture

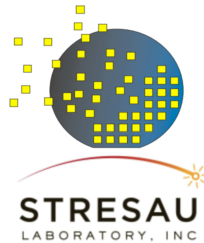


Key Milestone 2



- Small Business Gun Test

Outline



- Fabrication of Navy S&A Design
- Packaging
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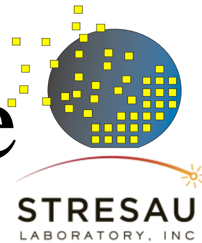
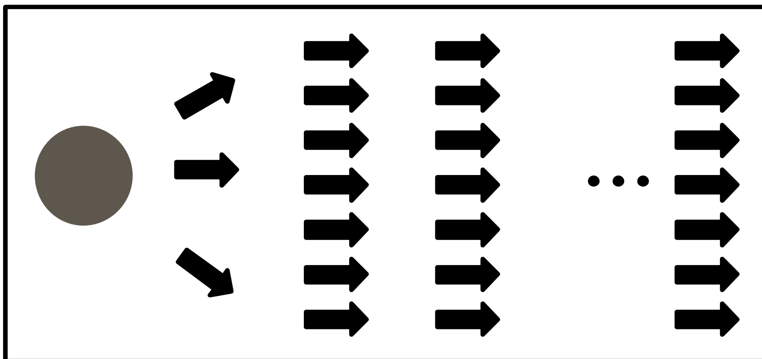
Low Cost Wafer Level Package

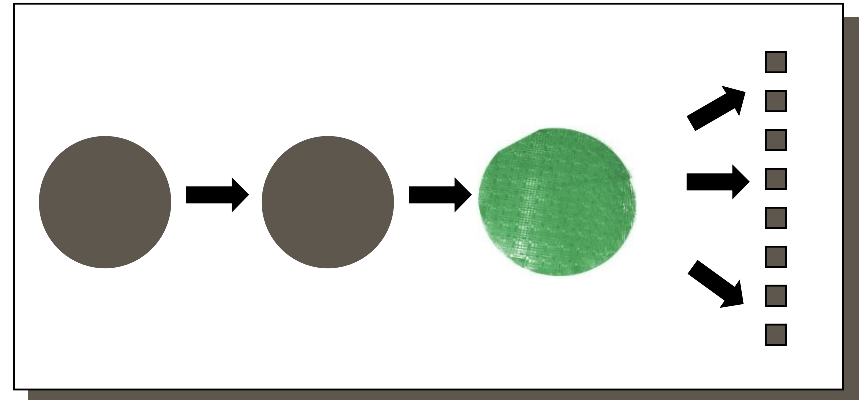


- Packaging is Expensive
  - Each Part Must Undergo Many Steps
- Unique Capability
  - Compatible with Energetic Materials
  - One Hundred Steps Instead of Tens of Thousands
  - Yield >90%: Reduce Cost by >10X

Conventional One-at-a-Time

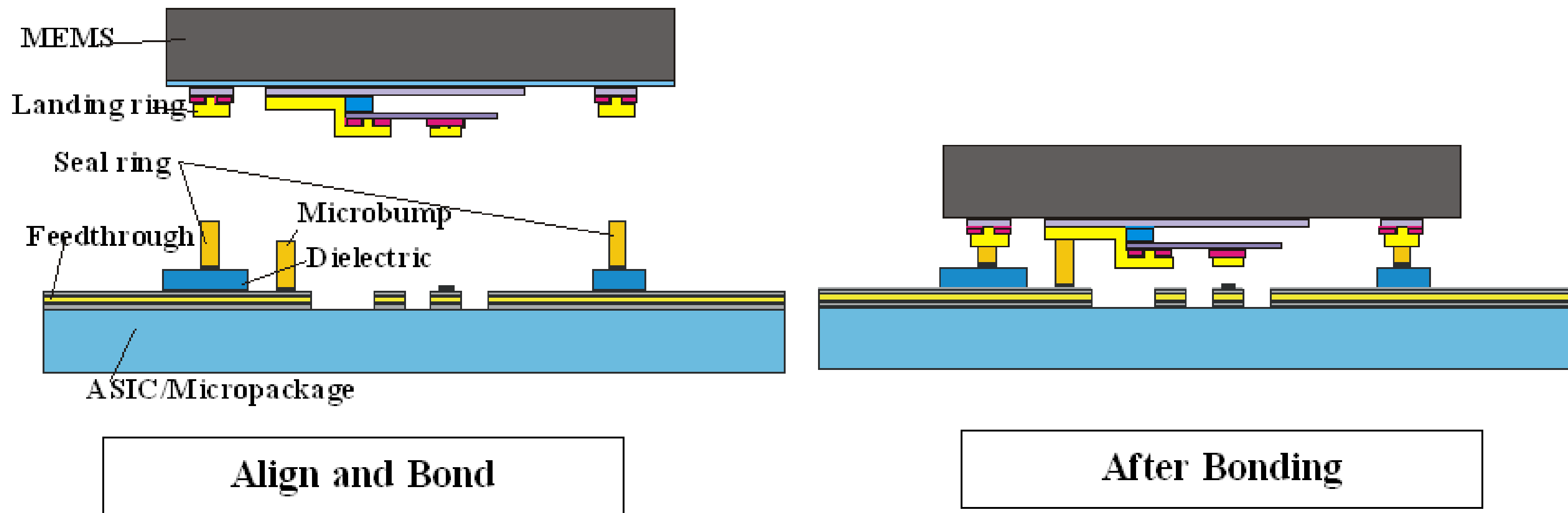


Our Solution: Thousands-at-a Time



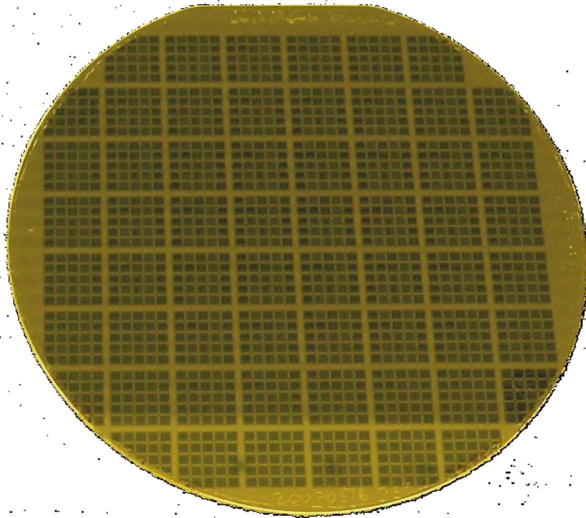
2-Substrate MEMS Process

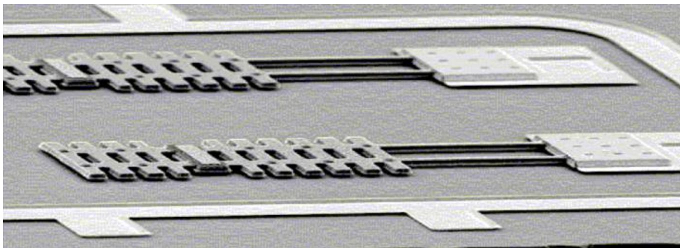
- Used in Many Device Designs
  - >90% Yield
  - Integrated Hermetic Packaging
  - Eliminates >80% of Production Cost



Wafer-Level Packaged Yield

- Initial Application: RF MEMS Switch

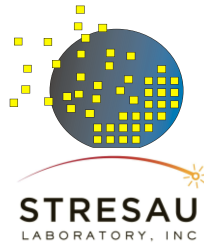


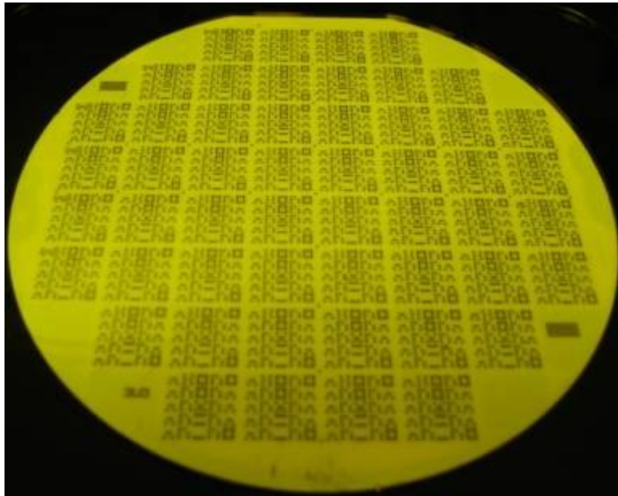


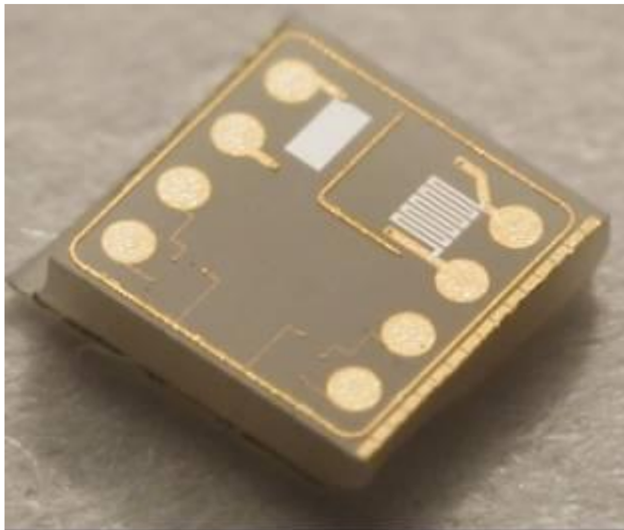
	Initial Run	Second Run*
# of Working Devices	98	117
Total # of Devices	192	136
Overall Yield*	51%	86%

*Process improvements were made and a second run was performed 3 months after the initial run.

Hermetic Packaging Yield

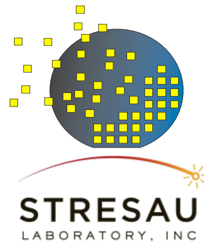






# of Hermetic Packages	45
Total # of Packages	50
Yield	90%

Outline



- Fabrication of Navy S&A Design
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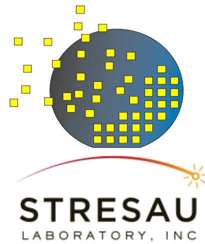
Processing Cost Estimate



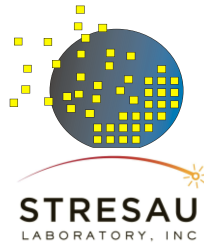
- Navy Cost Estimate
  - 500 Wafers per Year
  - 6” Wafer Size (MEMS Fab)
  - Small Scale Production
  - Goal: **$30 each**

MEMS S&A Chip Cost

Die Cost ($)	9 mm Die 69,000 units / year	7 mm Die 134,000 units / year	5 mm Die 277,000 units / year
Die Cost	$6.30	$3.25	$1.57

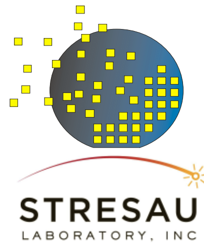
Y-axis: Die Cost ($), $0.00 – $7.00

Capacity



- 4” Pilot Line Q4 2010 – 45,000/year
  - 3 Wafers/Day (1 shift)
  - 300 Days/Yr
  - 250 Devices/Wafer (4” wafers)
- Simple 6” Manufacturing Line: 675,000/year
  - 9 Wafers/Day (3 shifts)
  - 300 Days/Yr
  - 250 Devices/Wafer (6” wafers)
  - Wafer bonder needs to be upgraded to 6”

Outline



- Fabrication of Navy S&A Design
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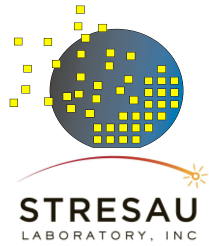
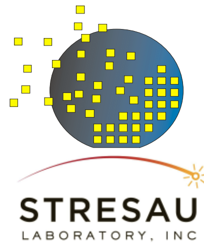
MEMS Production Cleanroom



- Cleanroom Qualified
- Equipment Set
  - DRIE Etch (4”, 6’)
  - Metallization (4”, 6”)
  - Lithography (4”, 6”)
  - Resist Coating (4”, 6”)
  - Resist Developing (4”, 6”)
  - Wafer Bonding (4”): 6” to be built
  - Dicing (4” and 6”)

Outline



- Fabrication of Navy S&A Design
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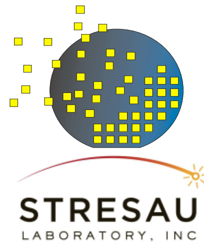
Next Steps



- Low Cost Scalable Production
  - Wafer-Scale 6” Ramp-Up
- Fuze Development
  - DoD Gun Tests
  - Explosive Train and Flyer
  - Battery/Power, G-Sensors, Control, …