Micro-machined High Density Embedded Capacitor Technologies for Energy Storage Applications

by

Thomas A. Baginski , Robert N. Dean, Michael Hamilton, John J. Tatarchuk and Aubrey N. Beal

Auburn University, Auburn Al

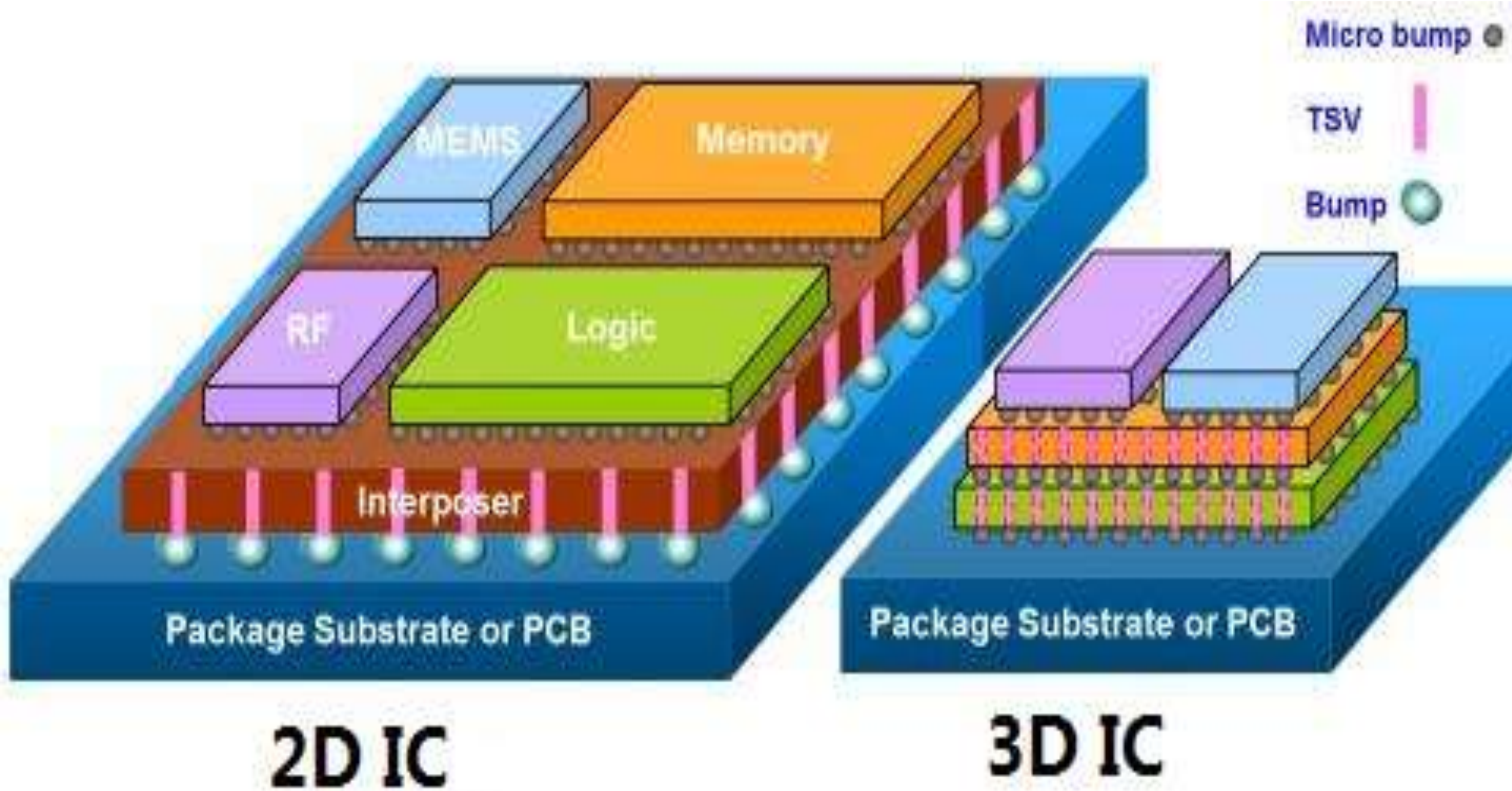
MEMS Super Capacitors: Application

- Substrate embeddable to provide current to circuits during power anomaly (i.e. Interposer)

- Requires low inductance path for rapid current discharge

- Requires etched cavities to increase surface area of capacitor

Interposer Provides Power Source Directly to Chips



Approach and Concepts

- Fabricate Planar Structure with SiO_2 (relative permittivity ~ 3.8)

- Fabricate Planar Structure with Atomic Level Deposition (ALD) HfO_2 (large relative permittivity ~ 25) from multiple vendors

- Fabricate Planar Structure with ALD HfO_2 and DRIE etched features

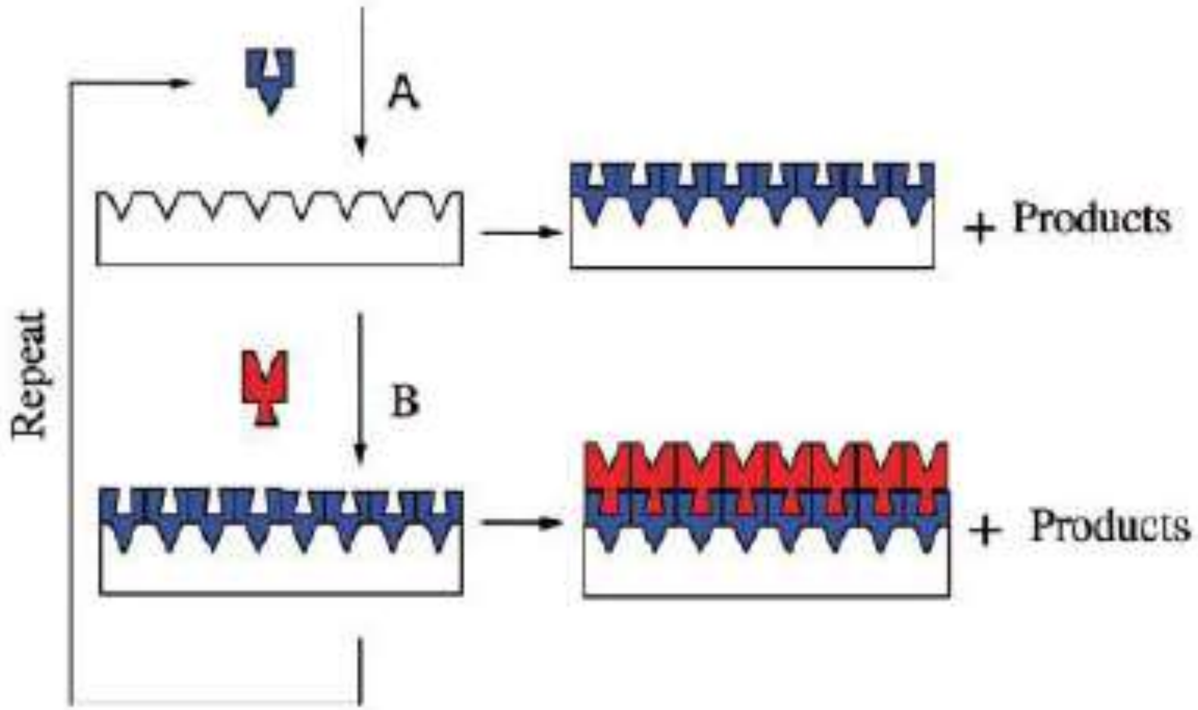
- Characterize Discharge Characteristics

- Summary

MEMS Super Capacitors: Fabrication

- n-type <100> silicon wafers
- Oxidized in steam/dry O_2 @ 1050° C for
  1- 4 hours $0.15\mu m < t_{ox} < 0.8\mu m$
- Top side selectively DRIE etched (increase surface area) and selectively doped
- Atomic Level Deposition performed
- Metalized with 100nm Ti /0.4µm of Cu

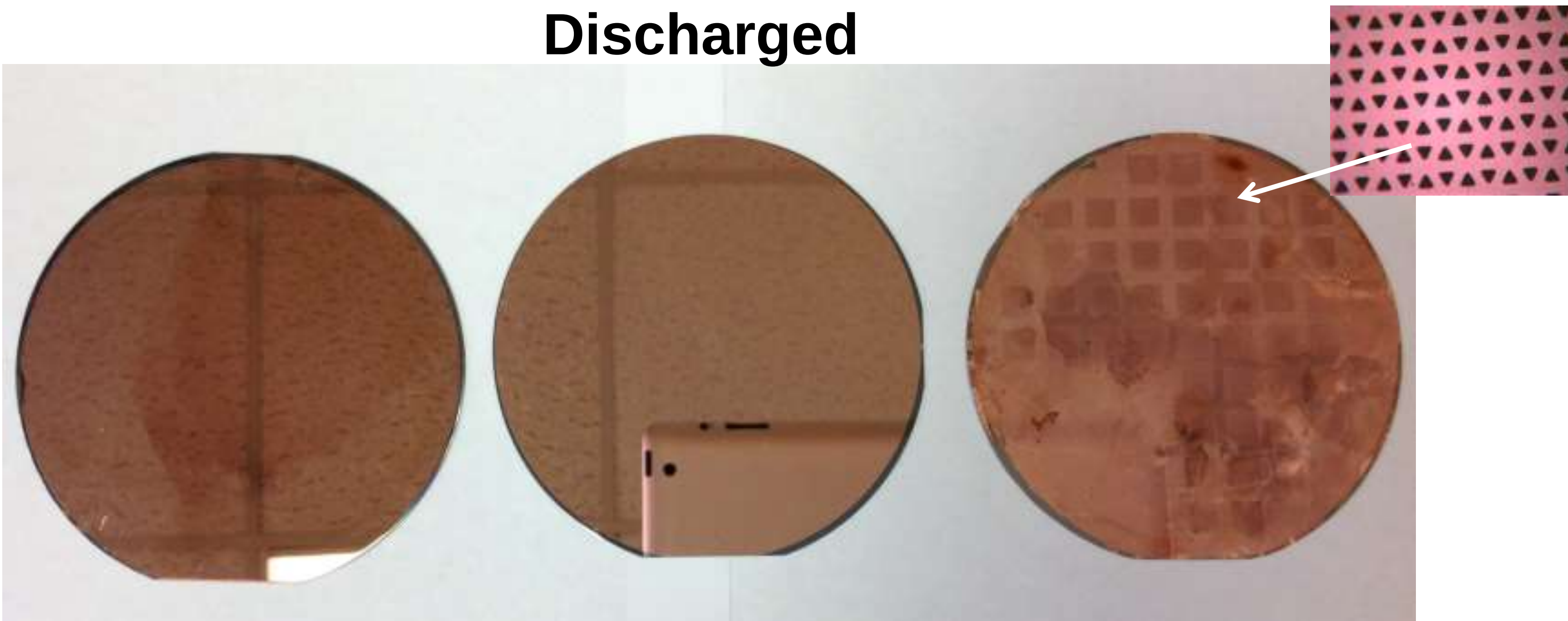
Basic Atomic Level Deposition Process



Interposer Capacitor 100 mm Silicon Test Wafers

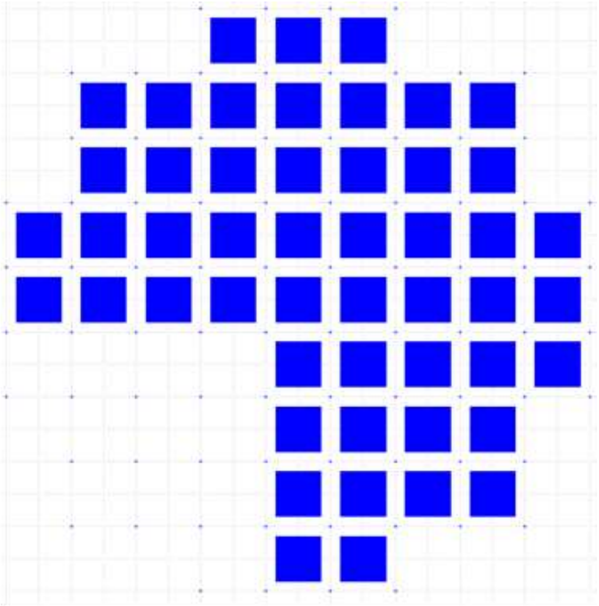
Thermal SiO_2 | ALD HfO_2 GIT | ALD HfO_2 Cam. Nano.

All Samples Initially Charged to 2V and then Discharged

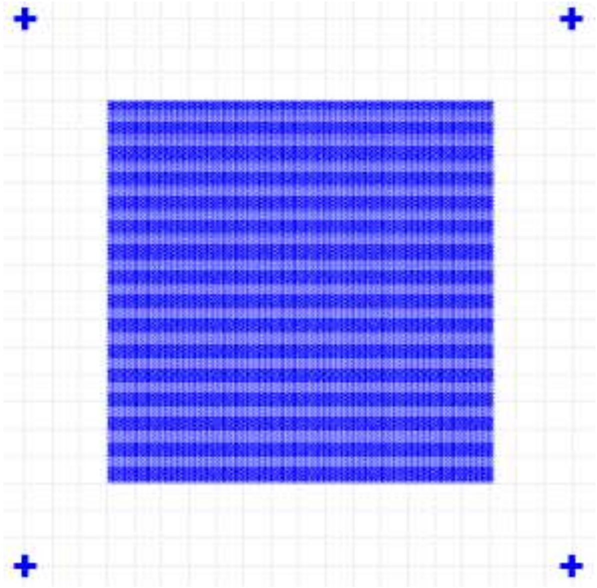


800nm | 3nm & 10nm | 30nm

MEMS Super Capacitors: Micromachining Pattern

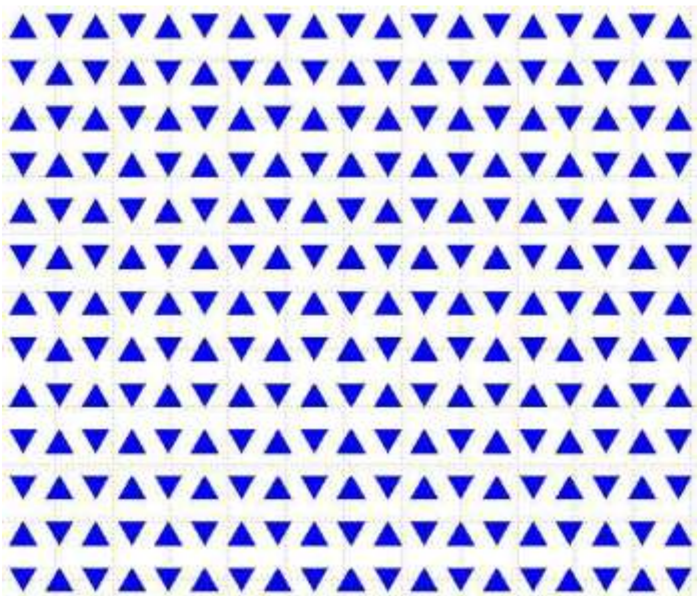


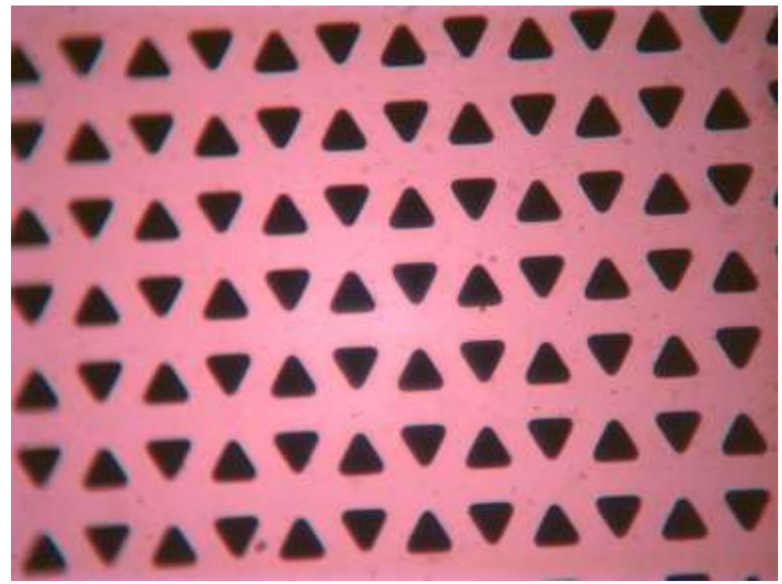
Layout of Wafer



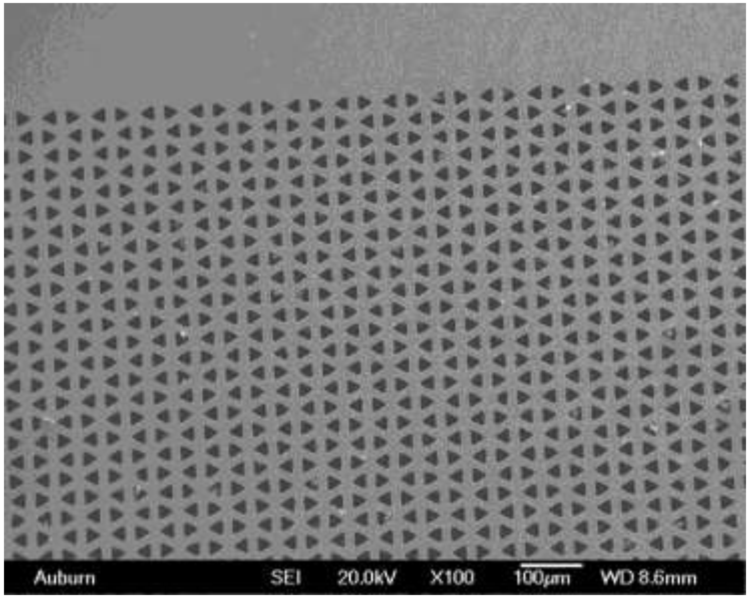
Layout of Individual Chip

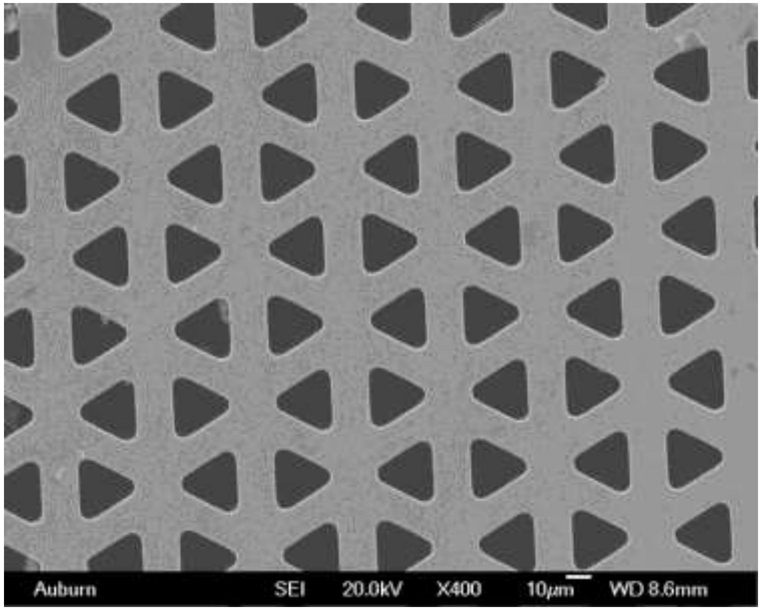
Cylinder and Triangle Pattern Utilized

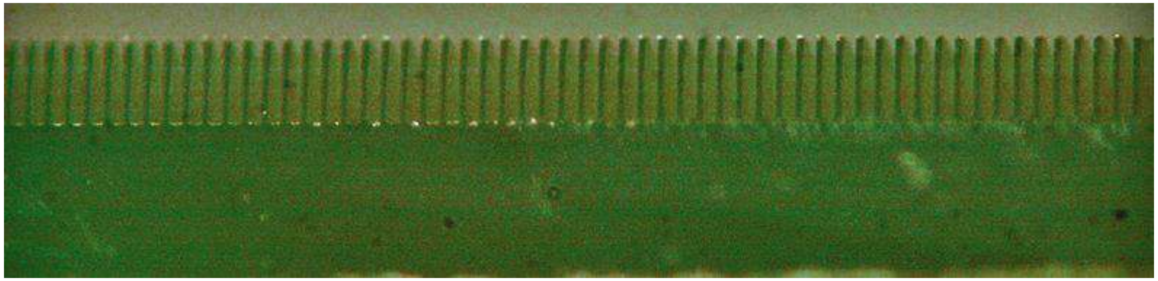




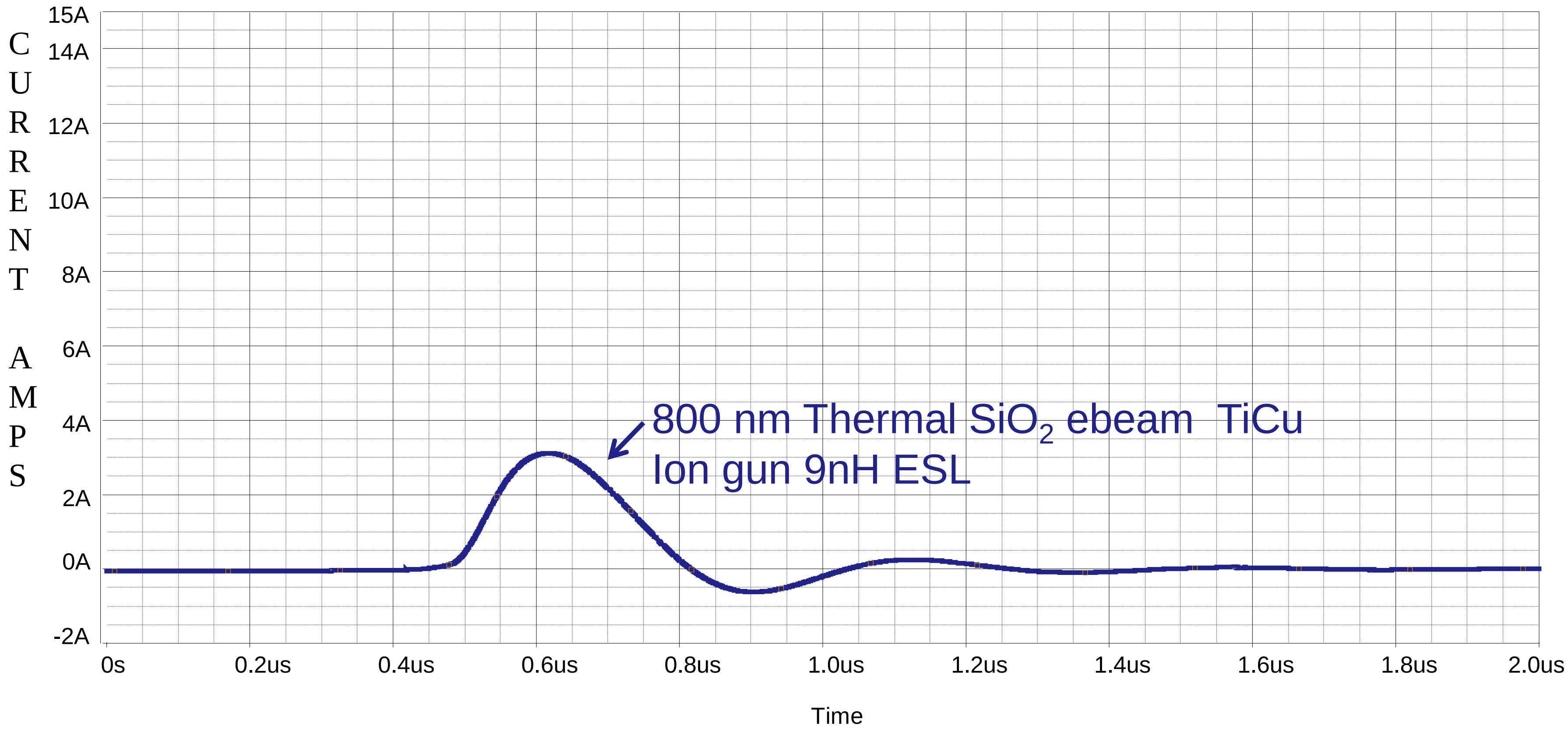
SEM & Photo Micrographs of DRIE Etched Features



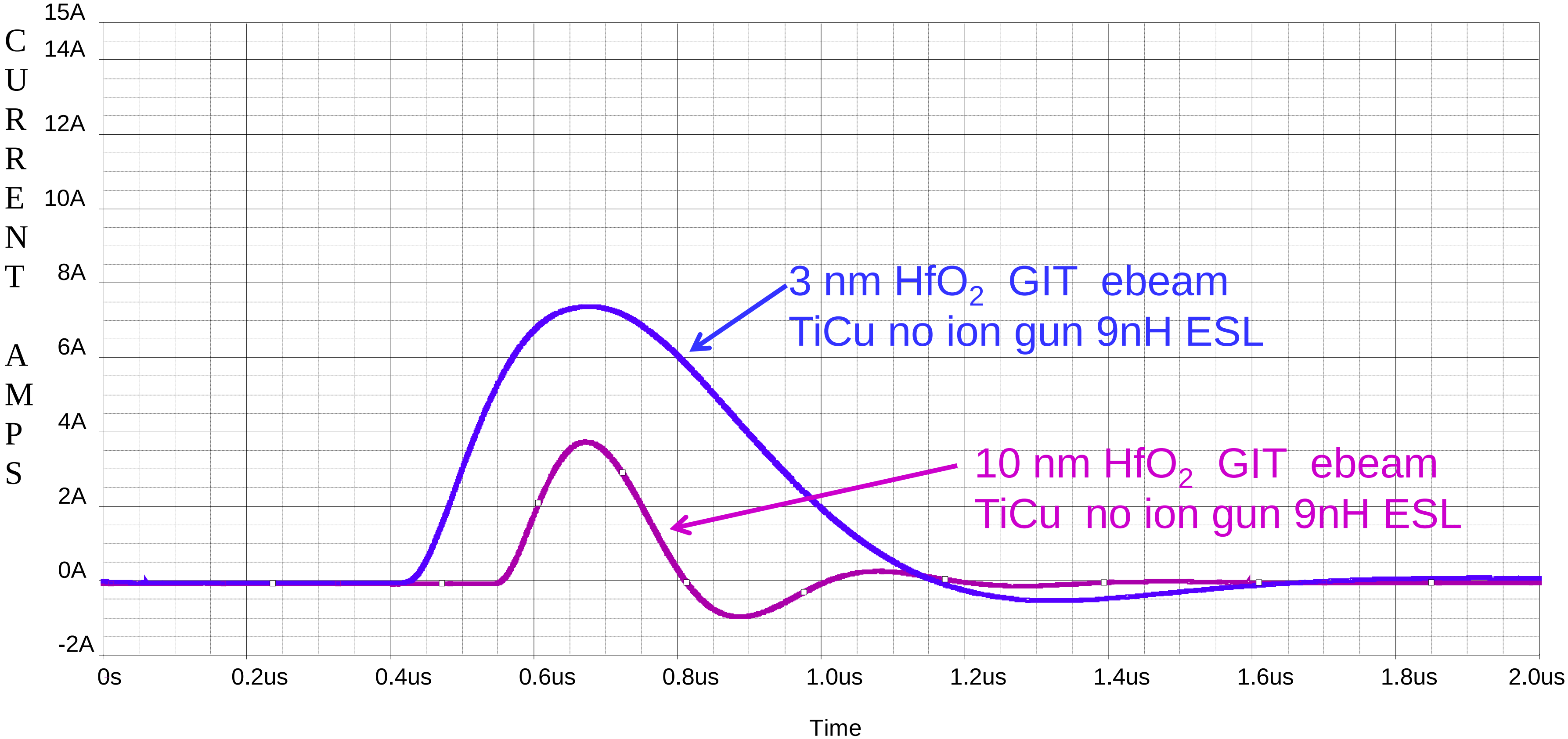




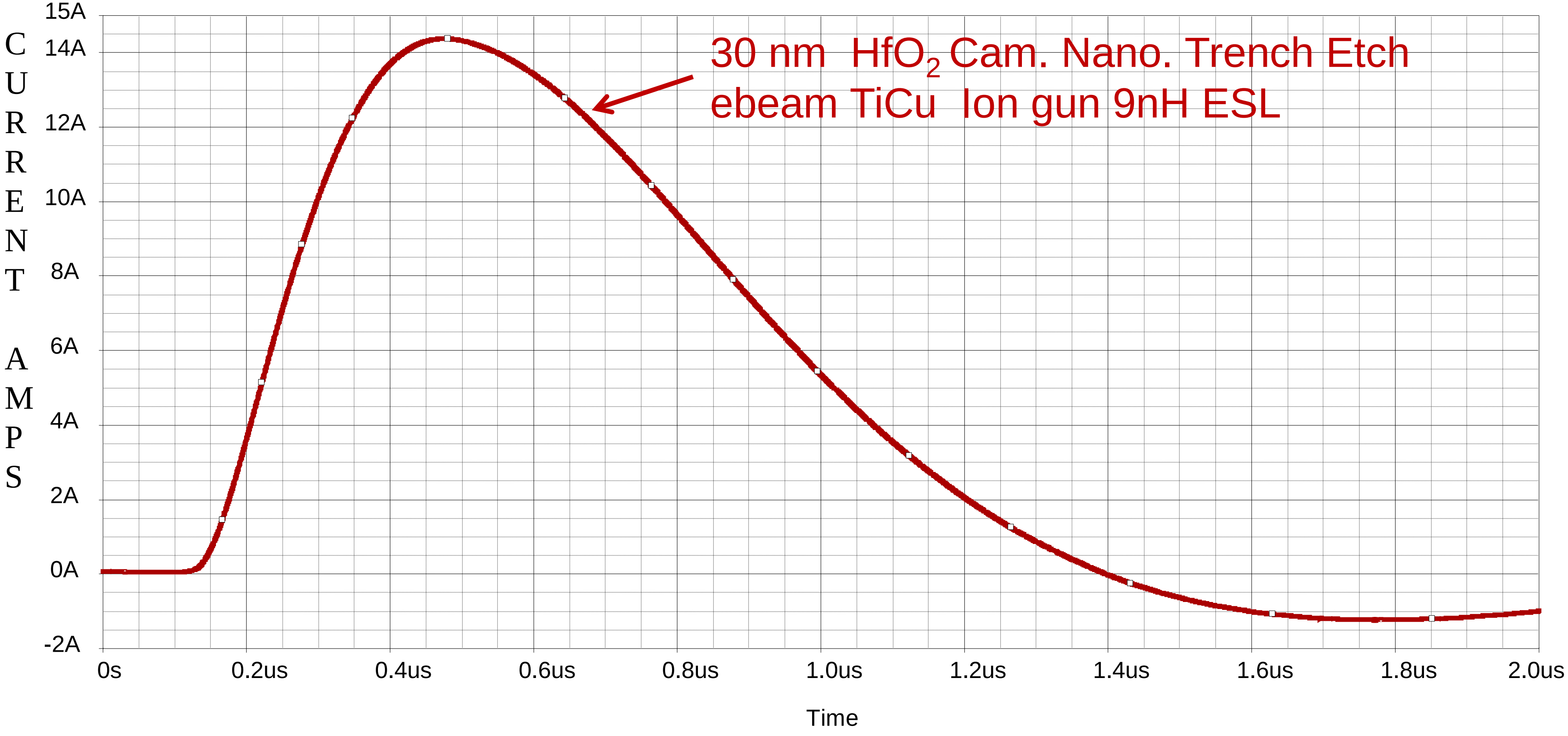
Thermal SiO_2 E-beam TiCu



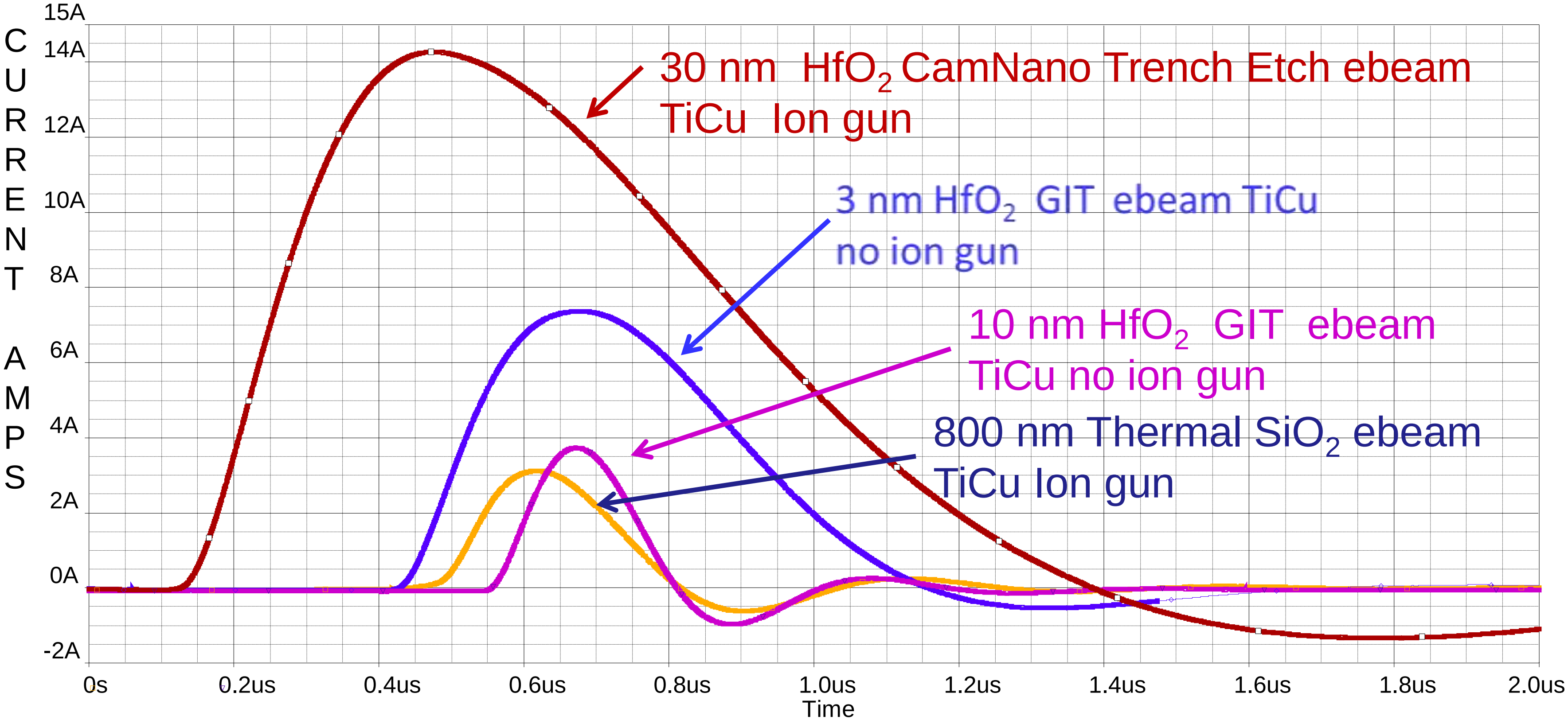
ALD HfO_2 GIT E-beam TiCu



ALD HfO_2 Cam. Nano. E-beam TiCu



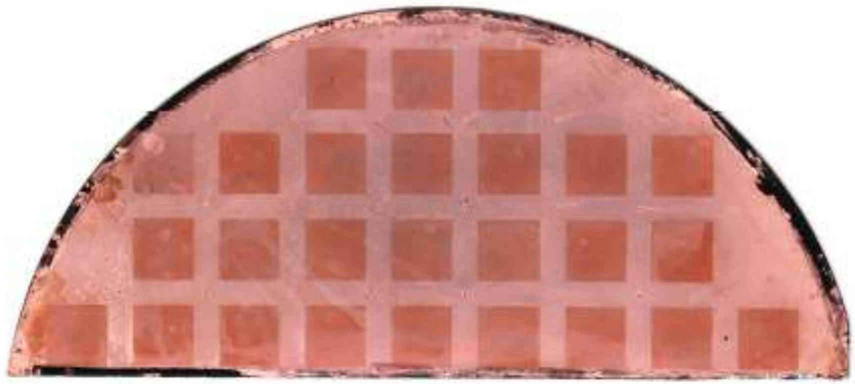
Composite



30 nm HfO2 CamNano Trench Etch ebeam
TiCu Ion gun
3 nm HfO2 GIT ebeam TiCu
no ion gun
10 nm HfO2 GIT ebeam
TiCu no ion gun
800 nm Thermal SiO2 ebeam
TiCu Ion gun
CURRENT AMPS
15A
14A
12A
10A
8A
6A
4A
2A
0A
-2A
0s
0.2us
0.4us
0.6us
0.8us
1.0us
1.2us
1.4us
1.6us
1.8us
2.0us
Time

Half Wafer HfO_2 Capacitor

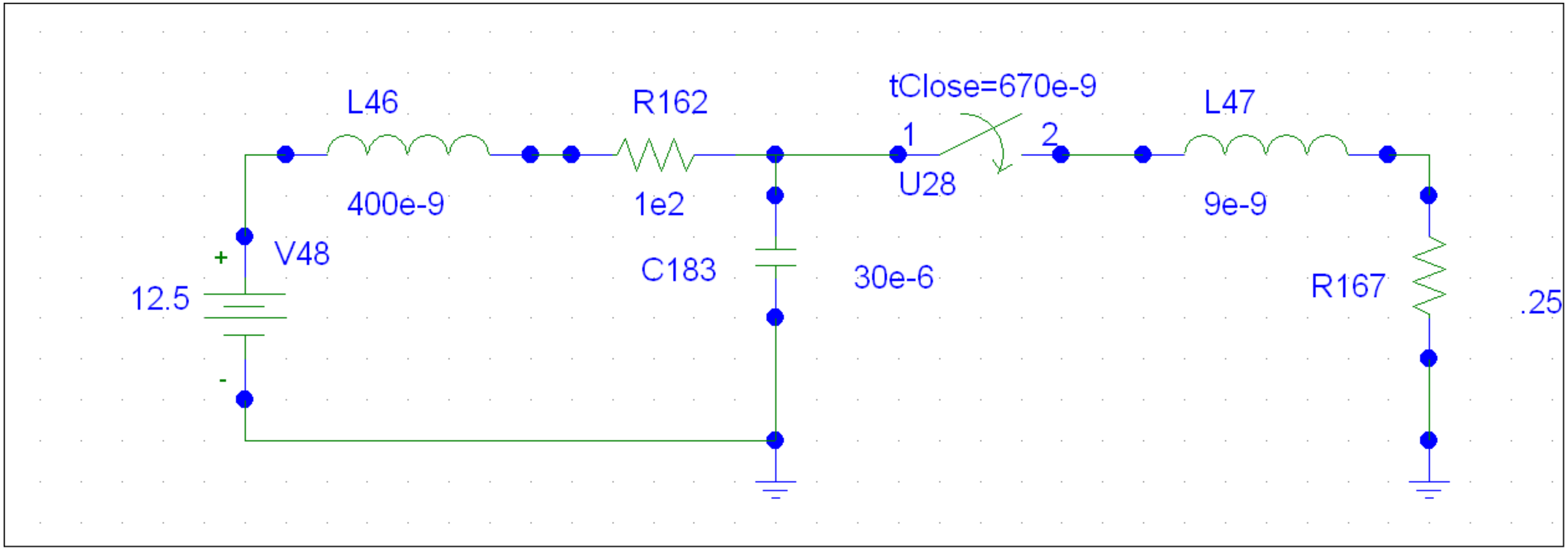
Sample Charged to 12.5V and then Discharged



$$C = (\varepsilon_R \varepsilon_o \text{Area})/t_o$$

$$C \sim 30{,}000\text{nF}$$

Test Circuit for Half Wafer HfO_2 Capacitor: 9nH ESL



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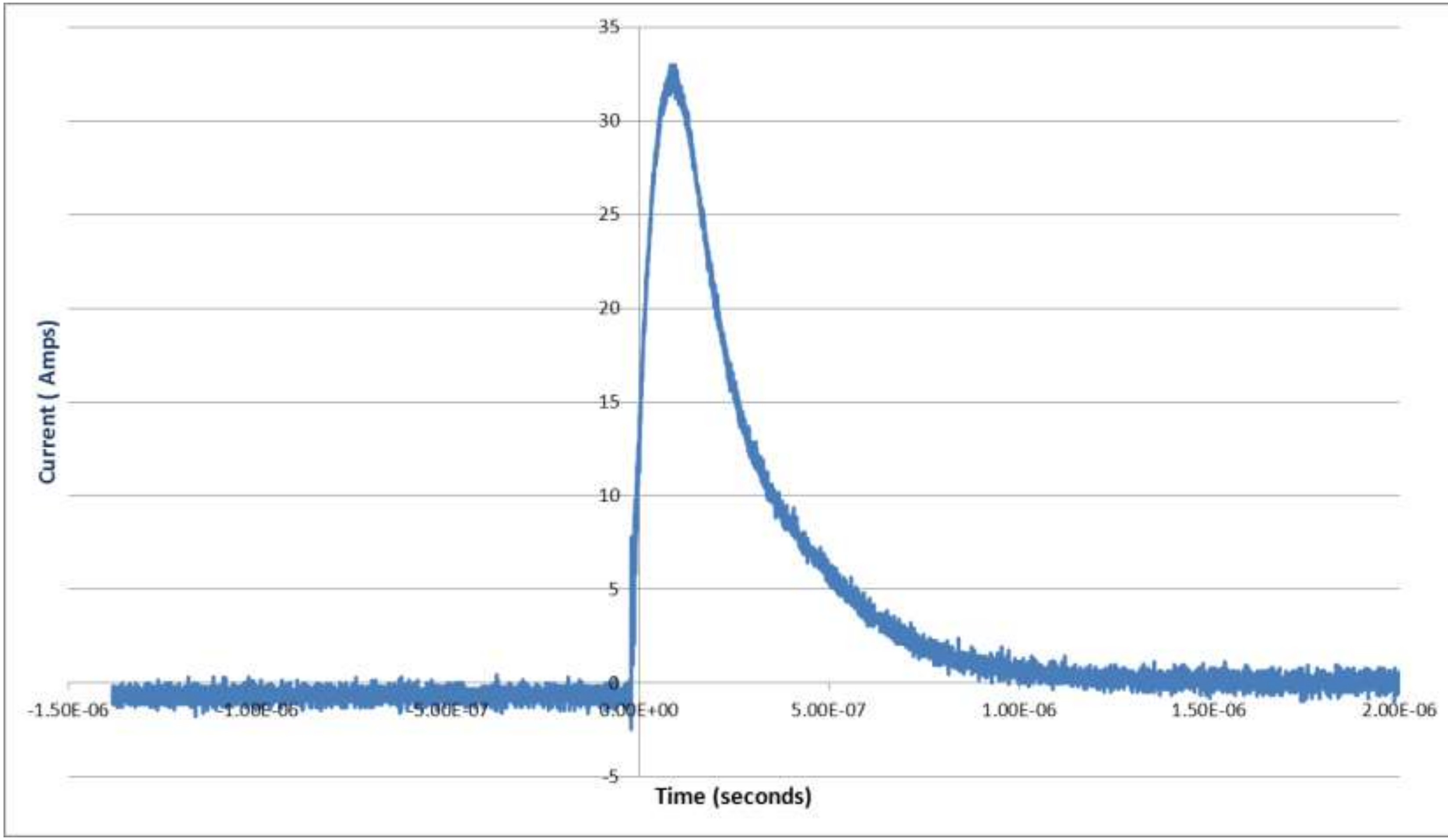
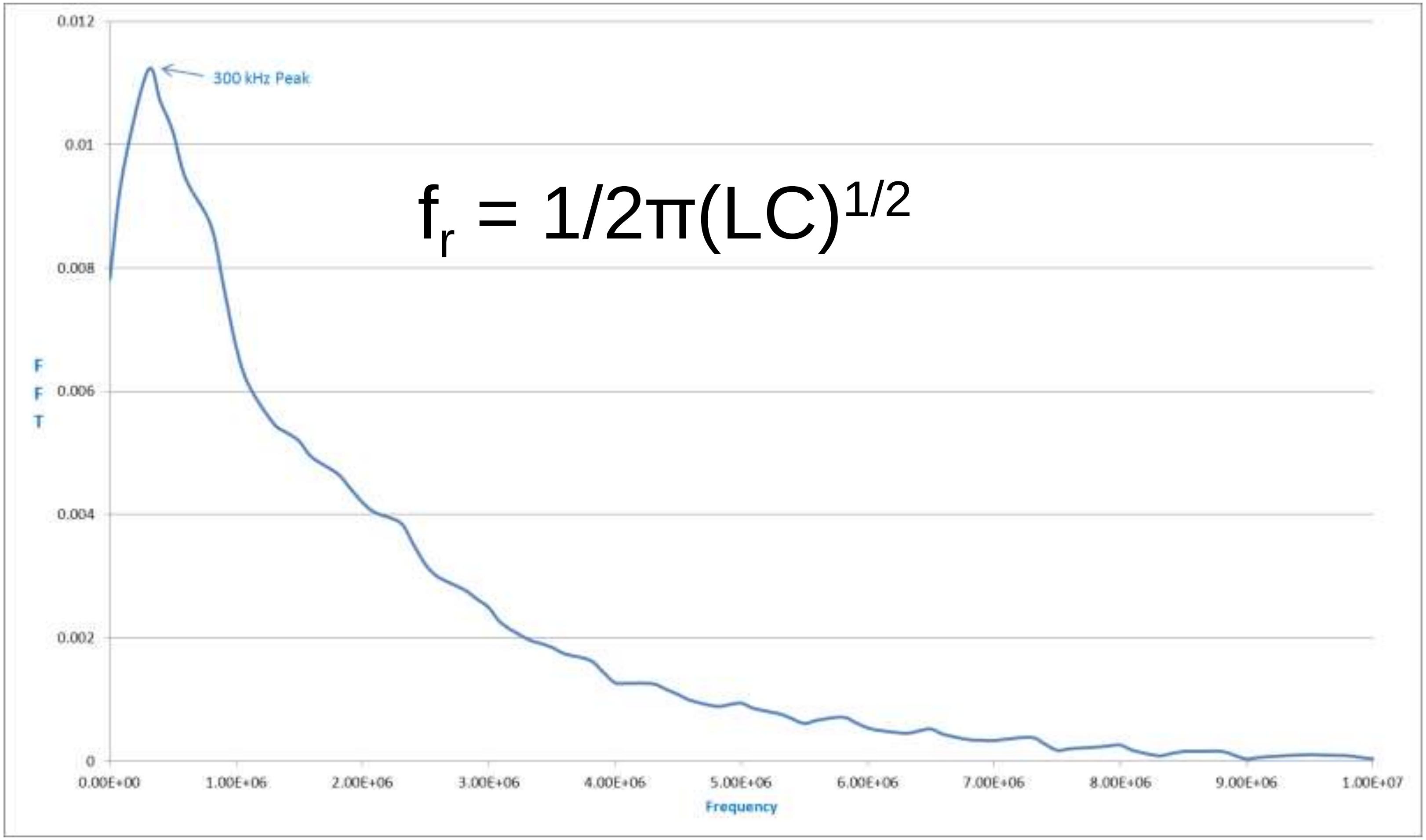
Ringdown in Time Domain

- 30nm thick hafnium oxide 30,000nF 12.5V discharge with an ESL = 9nH ESR = 0.25Ω



FFT of Ringdown

- 30nm thick hafnium oxide 30,000nF 12.5V discharge with an ESL = 9nH ESR = 0.25Ω

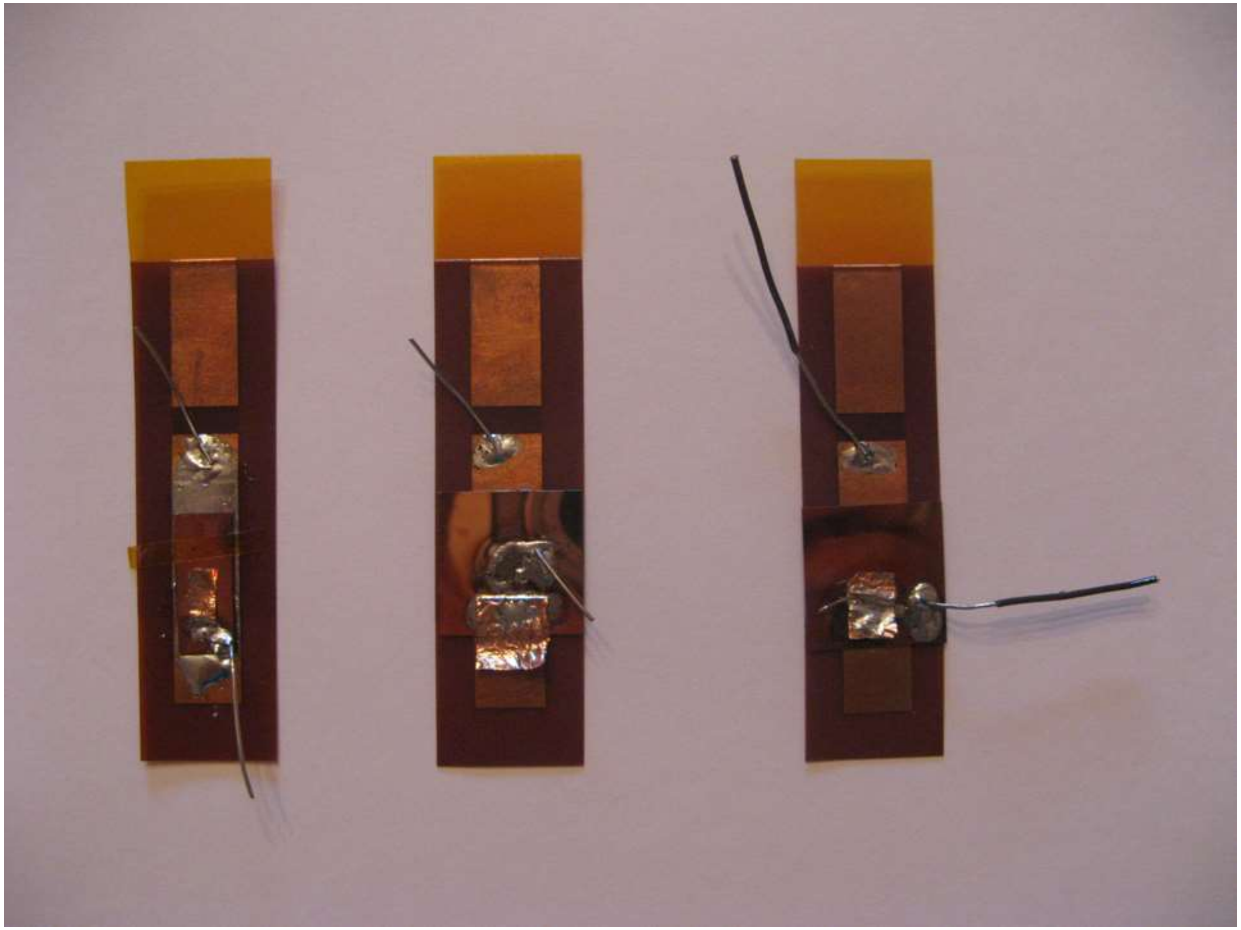


$$f_r = 1/2\pi(LC)^{1/2}$$

MEMS Super Capacitors: SPICE Modeling

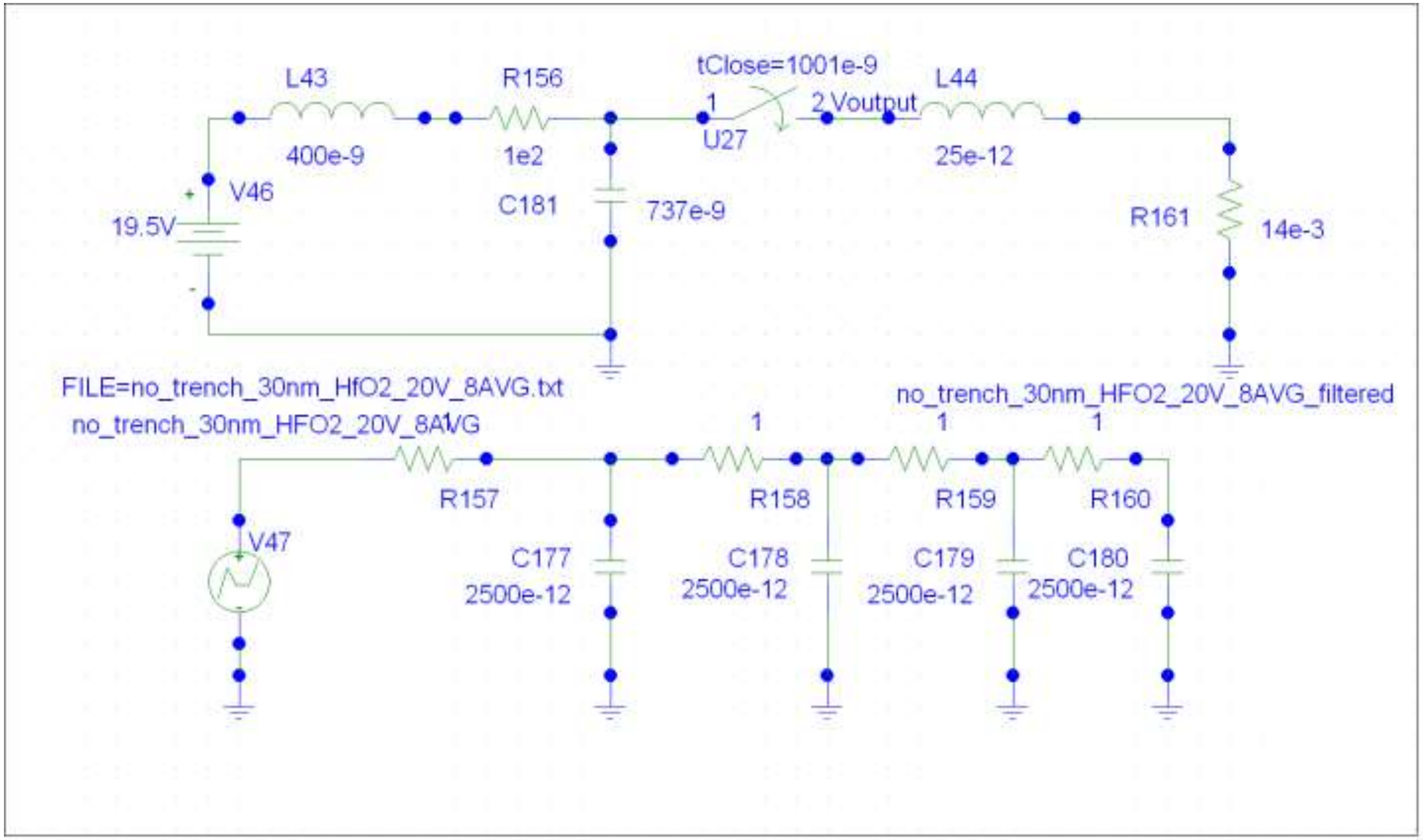
- High speed ringdown tests for a variety of configurations performed to determine capacitor performance under rapid discharge conditions
- Empirical data compared graphically to theoretical voltage discharge profiles
- Current discharge calculated from C(dV/dt)
- Results plotted and compared

MEMS Super Capacitors: Photos



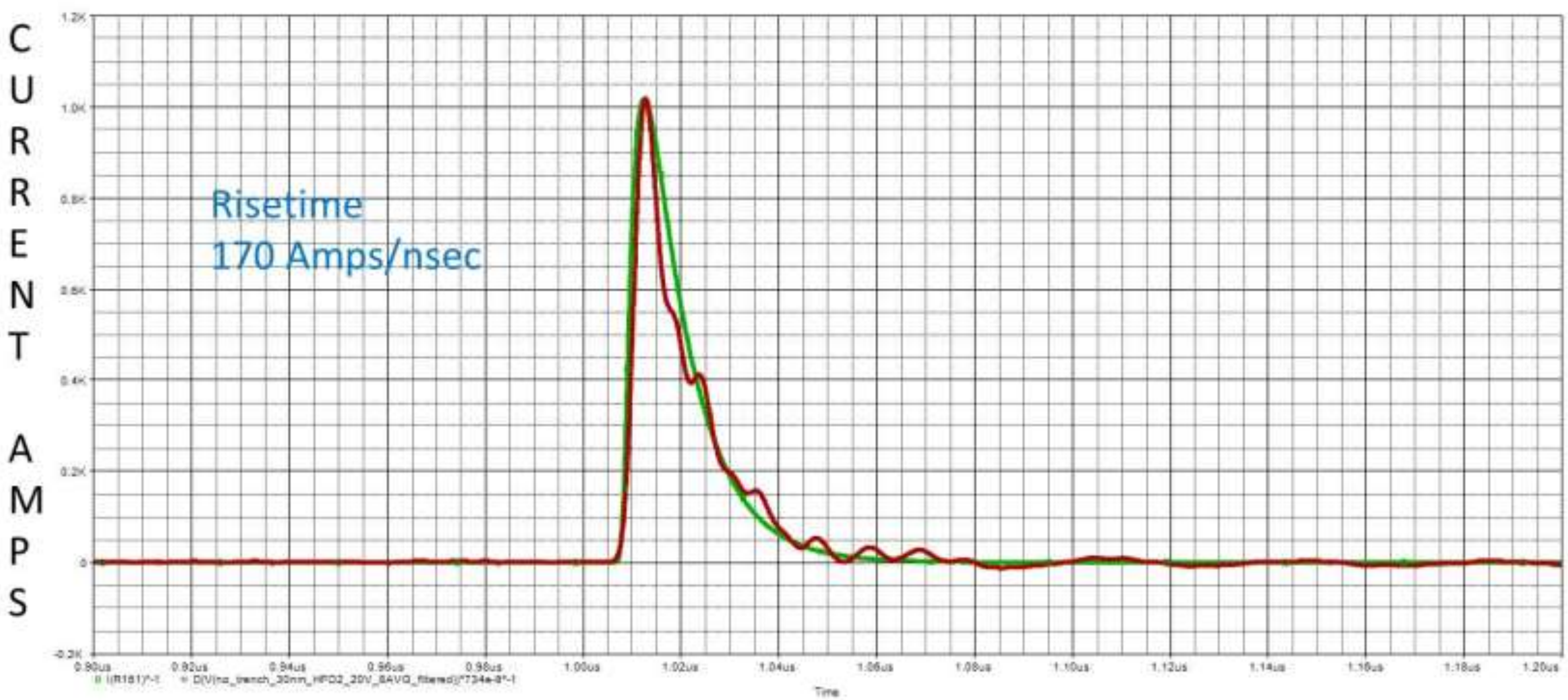
PSPICE Model

- 30nm thick hafnium oxide capacitor C = 734nF, 19.5V discharge voltage with an ESL = 25pH   ESR = 14mΩ



Ringdown in Time Domain

- 30nm thick hafnium oxide capacitor C = 734nF, 19.5V discharge voltage with an ESL = 25pH   ESR = 14mΩ



Summary

- Possible to fabricate high value capacitors for interposer

- Risetime dependent upon load

- HfO_2 has high dielectric constant (~25)

- SiO_2 is more readily available from silicon foundries