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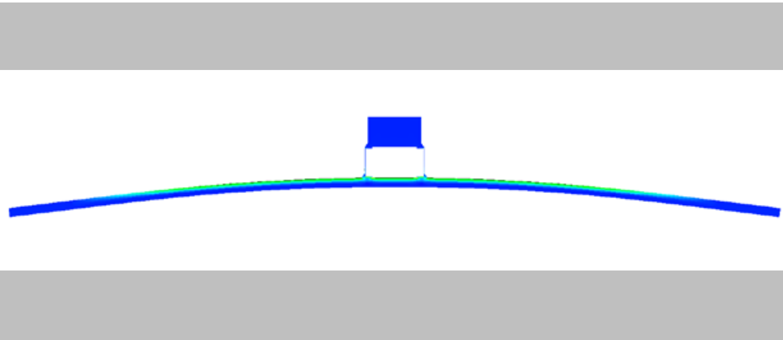

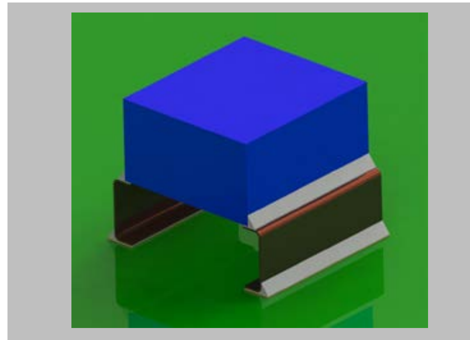

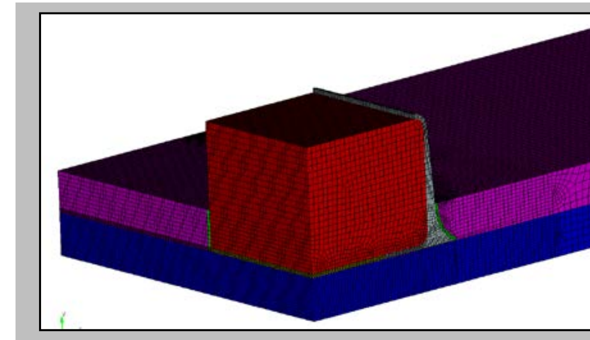

Evaluation of a Novel Mounting Method for Surface Mount Capacitors

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Sandia National Laboratories

NDIA 58th Fuze Conference, July 7th-9th, 2015

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U.S. DEPARTMENT OF ENERGY

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Outline

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- Introduction / Purpose
- Evaluation of Traditional Mounting Strategies
  - Finite Element Modeling
  - Lab Scale Testing
- Evaluation of New Copper Tab Mounting Strategy
  - Concept Overview
  - Finite Element Modeling
  - Lab Scale Testing
- Conclusions / Path Forward

Introduction / Purpose

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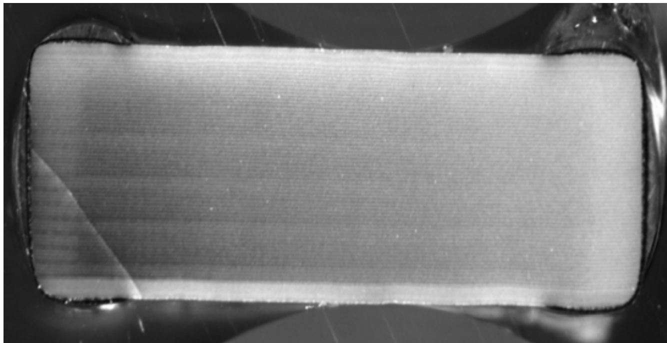
- Multilayer leadless ceramic chip capacitors (MLCCs) are a widely used type of surface mount technology (SMT) capacitor
- One prevalent failure mode involves cracking of the capacitor body due to printed circuit board (PCB) flexure.
  - Historical packaging strategies have included a “stress-relief” overcoat
- **Purpose:** **Look at historical packaging strategies and investigate *feasibility* of new mounting method using Finite Element Analysis (FEA) and lab scale experimentation**



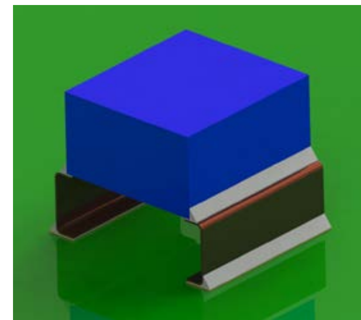
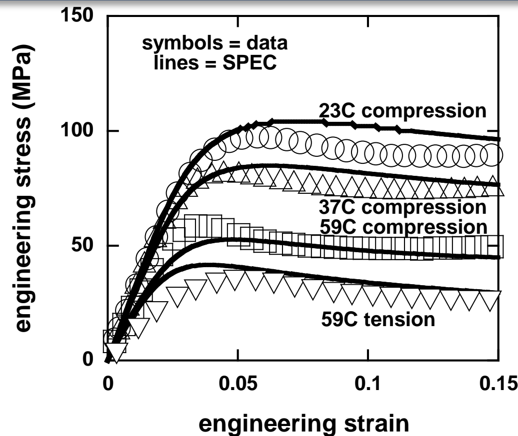


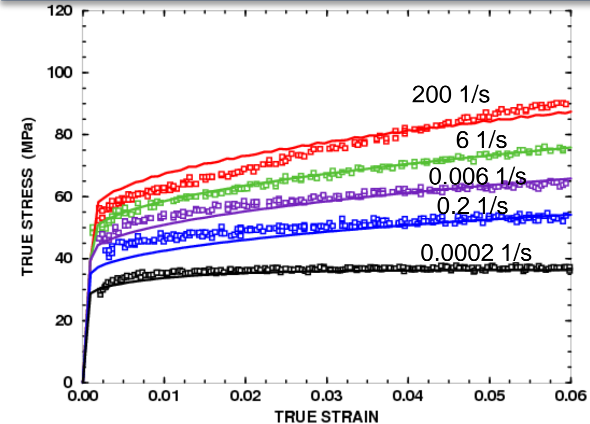
Image Source: N. J. Blattau, *Models for Rapid Assessment of Leadless Component Failures During Printed Wiring Board Bending,* University of Maryland, 2004.

FEA Material Models

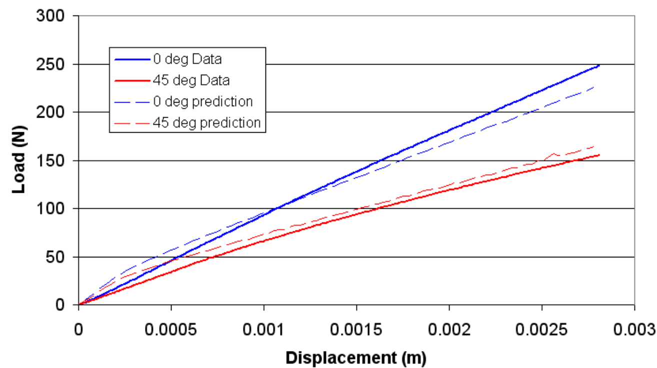
Potting
Nonlinear-Viscoelastic Model



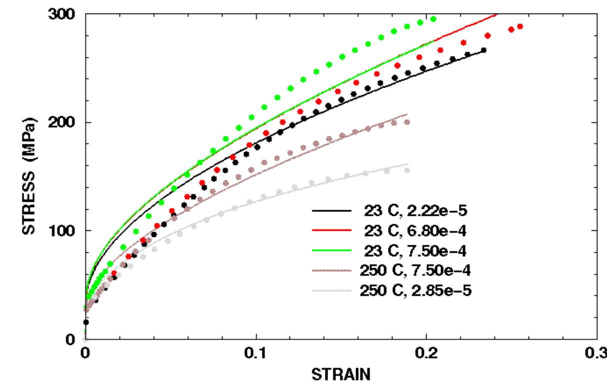
Sn-Pb Solder
Viscoplastic Model



FR-4
3D Elastic Orthotropic Model



Annealed OFHC Copper
Viscoplastic Model



Excellent material models for Potting, Solder, and FR-4. Copper data fit to slow strain rate data – needs improvement for higher strain rates.

Thermal Deflection Study – FEA

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Potting
Universal polymer model
- Reference temperature: 85°C
- Stress free temperature: 70°C
- Filler volume fraction: 0.0001

PCB
FR4 elastic 3d orthotropic model

Capacitor
Ferrite elastic model

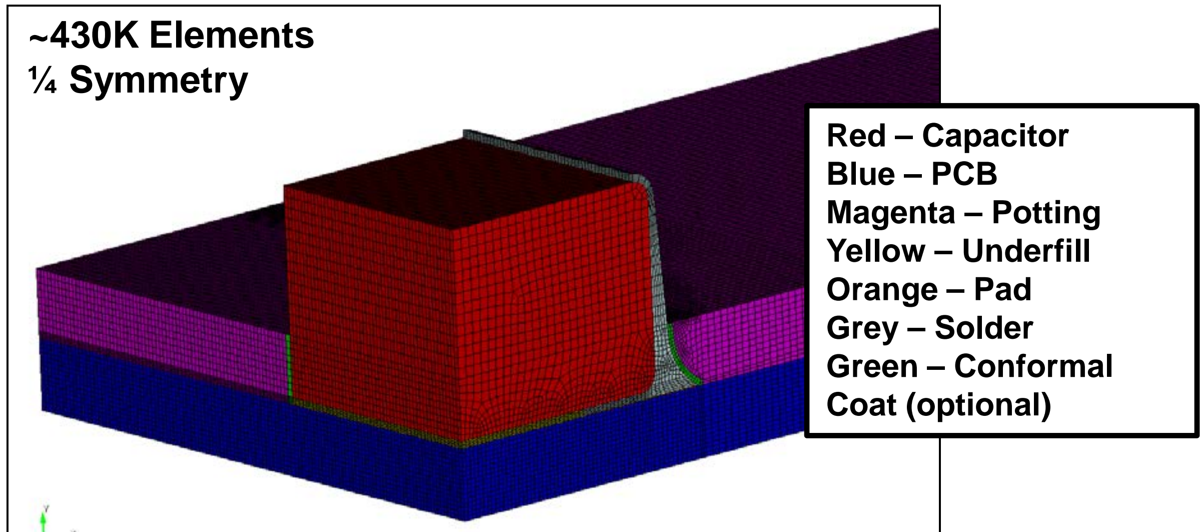
Solder
Sn-Pb viscoplastic model

Pad
Copper elastic-plastic power-law hardening model

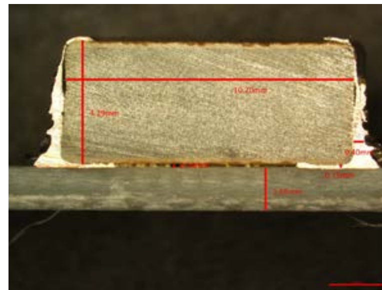
Conformal Coats
Phenolic microballoon (PMB) filled polysulfide mooney rivlin model

Underfill (hard)
Universal polymer model
- Reference temperature: 80°C
- Stress free temperature: 80°C
- Filler volume fraction: 0.2

Geometry
Capacitor - 0.4” x 0.17” x 0.4”
PCB - 1.0” x 0.058” x 3.0”
Coat Thickness – 0.005”
Potting thickness - .056”



Experimental Cross-Section



Case	Underfill	Conformal Coat
Case I	Yes	No
Case II	Yes	Yes
Case III	No	Yes
Case IV	No	No

Thermal Deflection Study – FEA

Thermal Cycles

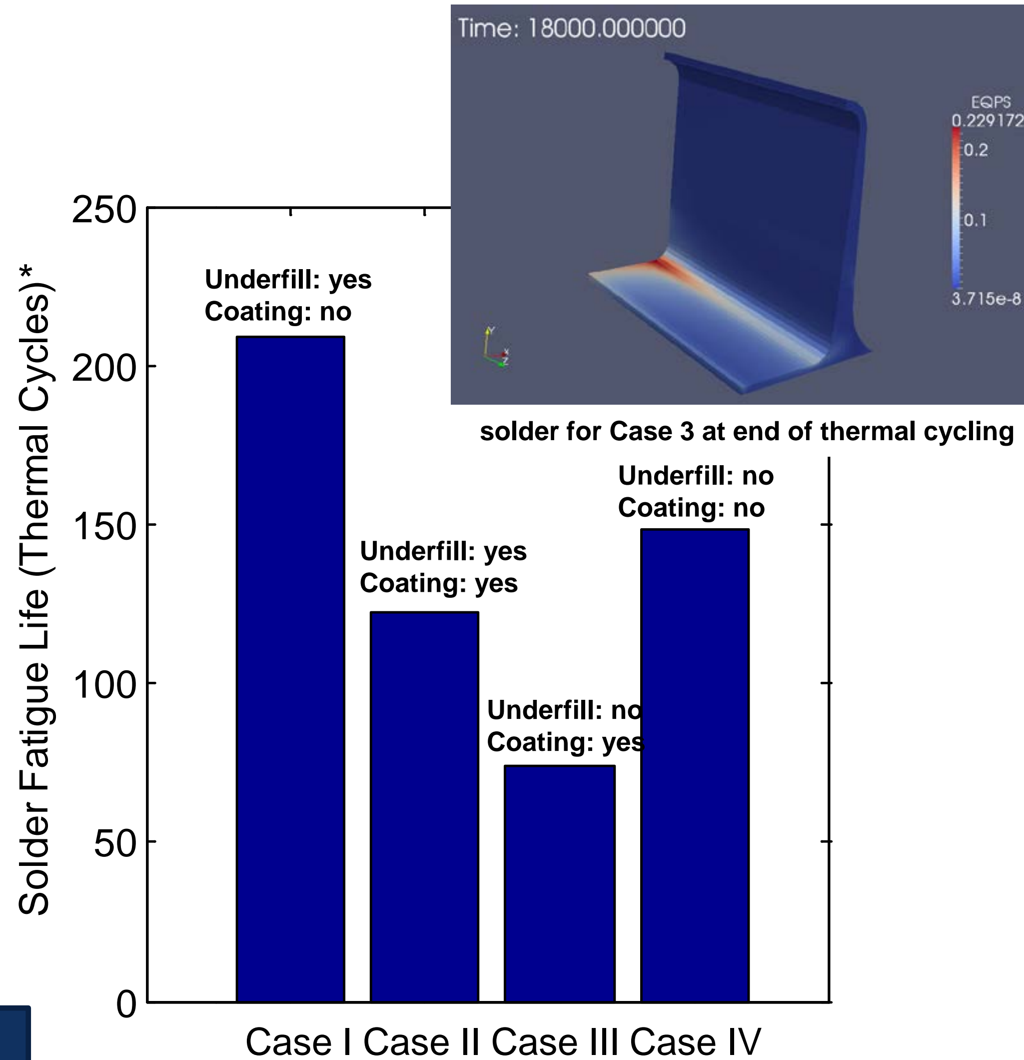
- 3 cycles from 70°C to -55°C
- Each leg takes 1 hour

Analysis

- Equivalent plastic strain (EQPS) of solder compared at bottom of each thermal cycle
- Change in maximum EQPS from 3rd cycle used in Coffin-Manson criterion to estimate solder fatigue crack initiation

$$N_f = \left(\frac{1.31636}{\Delta EQPS} \right)^{1.96078}$$

Underfill Good, Coating Bad.



*Maximum EQPS is in same location for all cases

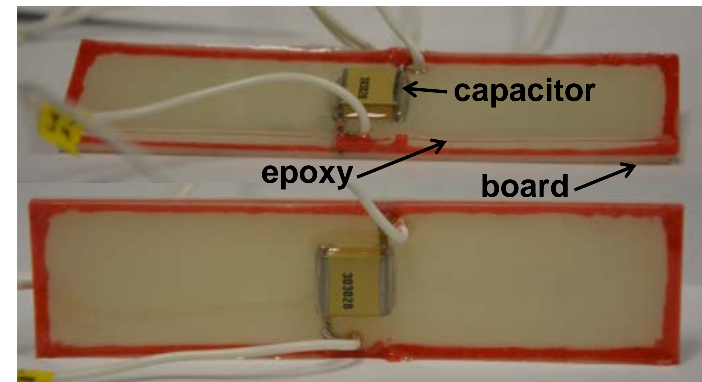
Thermal Deflection Study - Experiment

Sandia National Laboratories

- Experiment performed by colleagues at Sandia National Labs
  - Jamie Kropka, Lindsey Hughes, Haoran Deng, Mark Stavig, Carlton Brooks, Shelley Williams
- Experimental Summary
  - Board Material: 60 mil FR408
  - Capacitor: Novacap R2D, part# 4040R174K142PX (approximate dimensions 0.4”x0.4”x0.2”, LxWxT)
  - Samples packaged in different ways – with/without Underfills and Coatings
  - Thermal cycled (~1500 cycles in this case) between T=-50C and T=70C to induce board flexure
  - In-situ monitoring of device capacitance and board flexure (via strain gauge on bottom of board underneath capacitor)
  - Cross-sectioning and imaging of samples after thermal cycling

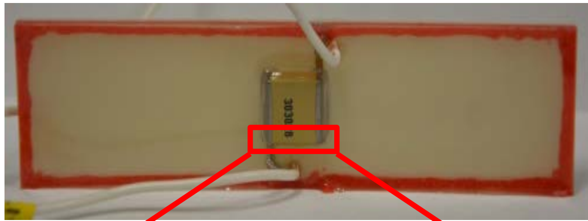
Asymmetrically Potted Capacitor-on-Board

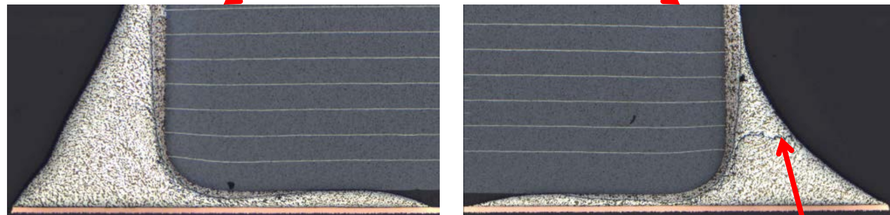
potting on one side of board induces flexure upon thermal changes



After ~1500 cycles…

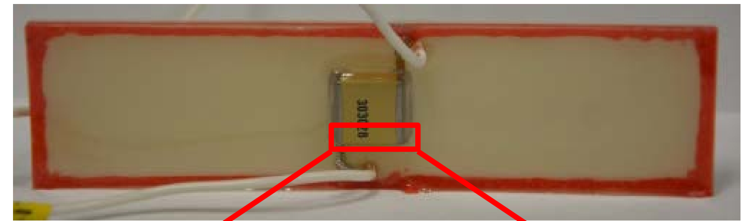
No Coating, Underfill

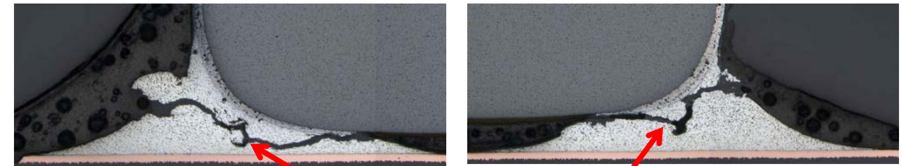




solder crack

Coating, No Underfill*





solder crack

Only samples with overcoat exhibit large gap solder cracking.

* markings to distinguish underfill operation were removed during coating process and samples must be further sectioned to confirm underfill state

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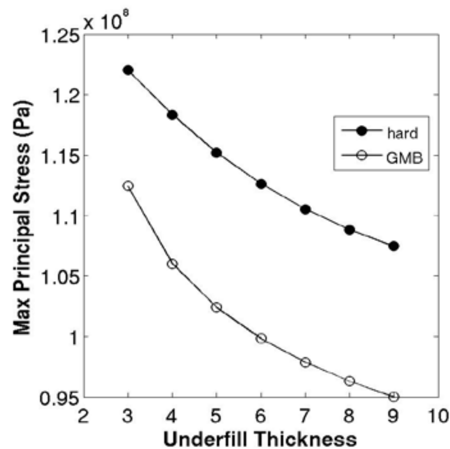
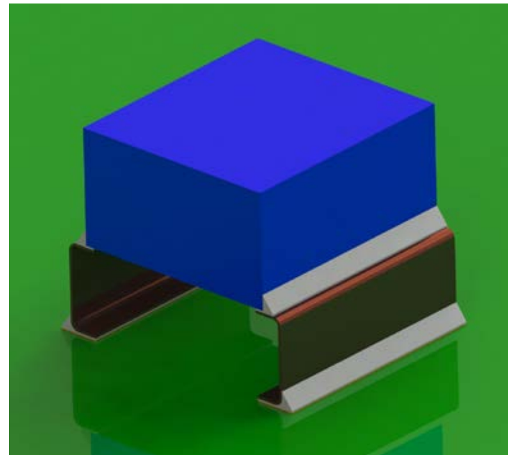
Underfill good

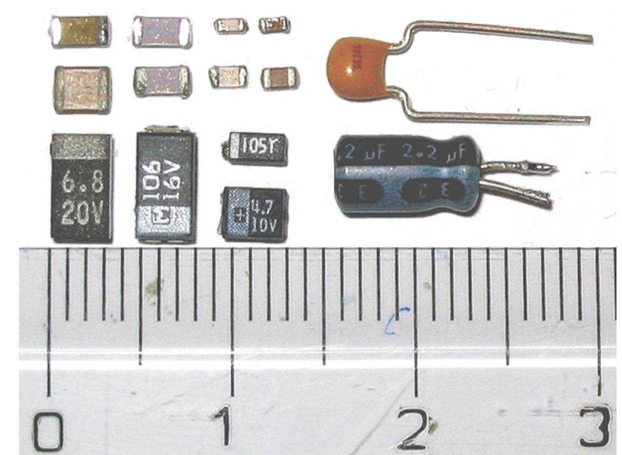
Overcoat bad

New Mounting Concept

- Previous study** has shown that thicker underfill thickness results in lower capacitor principal stresses
- Let’s try elevating the capacitor off of the board…much like the through-hole, leaded mounting methods







* Right Capacitor Image Source: Wikipedia.
** Neidigk, M., and Chambers, R., *Packaging Strategies for Printed Circuit Board Components Volume II: Component Studies,* SAND2015-0384, Sandia National Laboratories, Albuquerque, NM.

A word about Compliant Mechanisms…

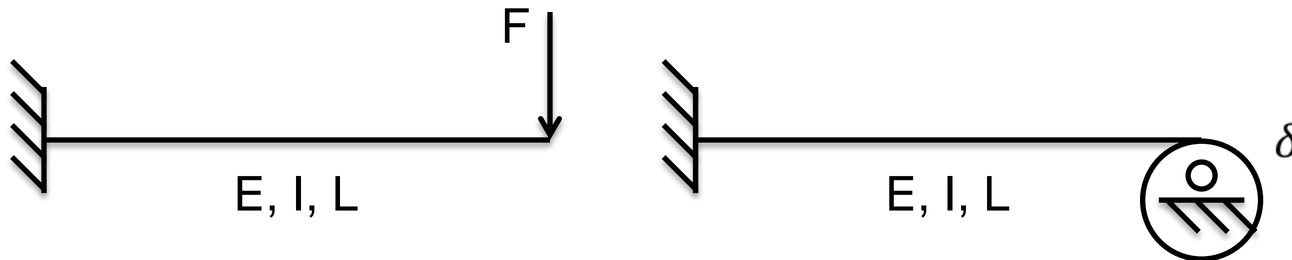
- Stiffness ≠ Strength
- Force Load:
  - $\sigma_{max} = \frac{M_{max}y}{I} = \frac{\mathrm{FLy}}{\mathrm{I}}$

    Reduce σ by increasing I, decreasing L
- Displacement Load:
  - $\delta = \frac{FL^3}{3EI} = \frac{M_{max}L^2}{3EI} \rightarrow M_{max} = \frac{3\delta EI}{L^2} \rightarrow \sigma_{max} = \frac{3\delta Ey}{L^2}$

    Solve for M

    Sub into σ

    Reduce σ by increasing L, decreasing E & y



Hypothesis: Long, thin tabs will reduce stress in capacitor.

Derivation from Howell, L., *Compliant Mechanisms*, John Wiley & Sons, 2001.

FEA Mesh/Perturbations

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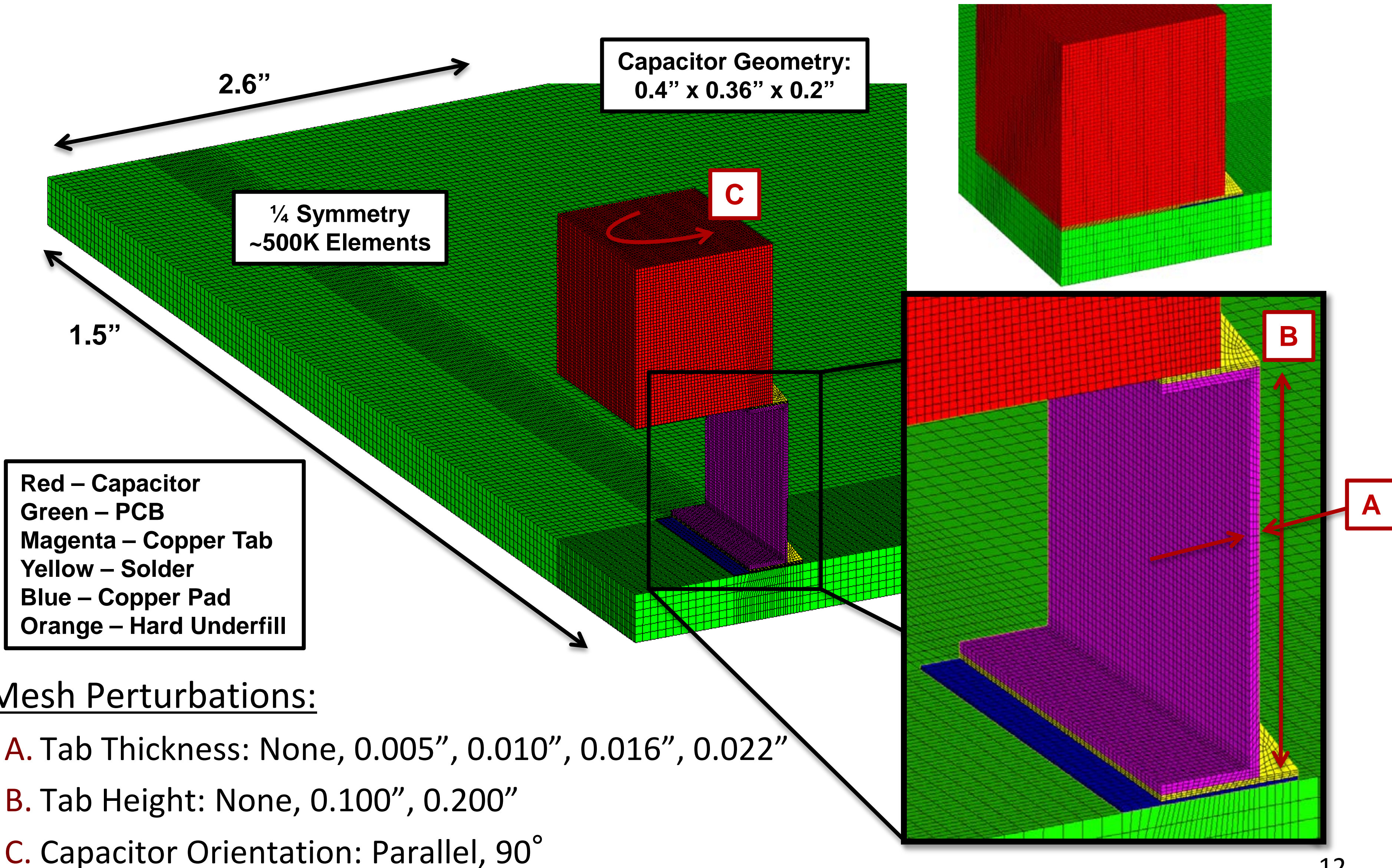

Mesh Perturbations:

A. Tab Thickness: None, 0.005”, 0.010”, 0.016”, 0.022”

B. Tab Height: None, 0.100”, 0.200”

C. Capacitor Orientation: Parallel, 90˚

FEA Procedures

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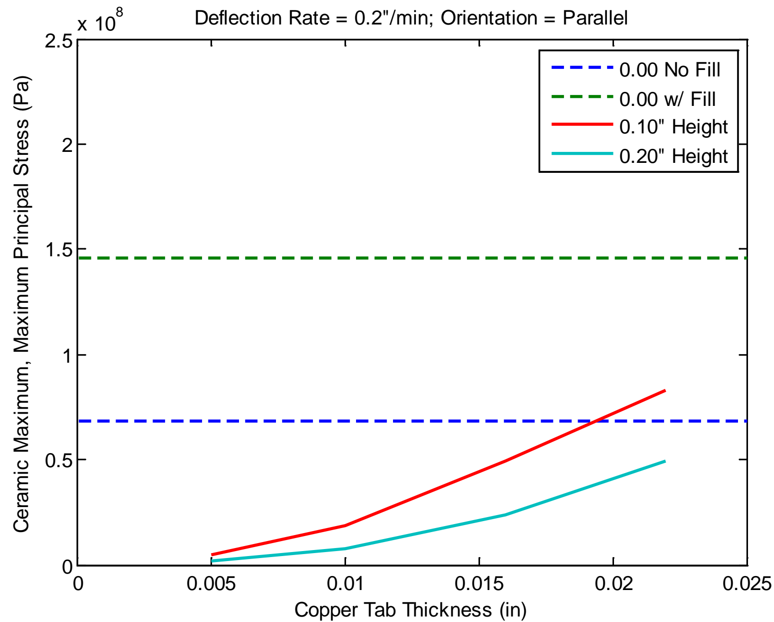
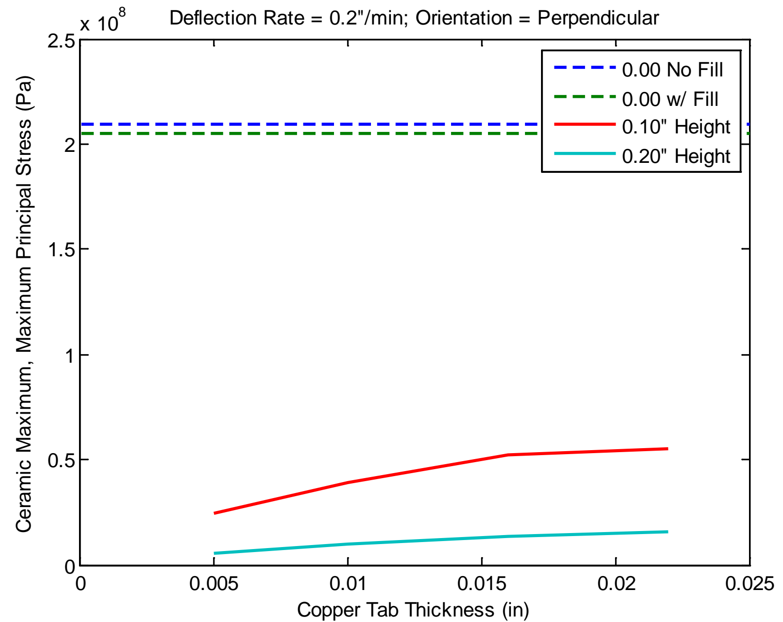
- JESD22B113 – JEDEC Board Level Cyclic Bend Test Method
  - 4 Point Bend Test w/ 75mm and 110mm spans
  - 2mm deflection, back to 0, and return to 2mm.
- Deflection performed at various rates
  - 20”/min., 2”/min., 0.2”/min., 0.02”/min.
- If Potting/Underfill used, thermal cycle applied to simulate cure process
- Analysis performed using Sierra Adagio* - 3D Nonlinear Solid Mechanical Finite Element Application

* Sierra/SM Development Team, *Sierra/SM 4.32 Verification Tests Manual*. SAND2014-3257. Albuquerque, NM, 2014.

FEA Results

- Capacitor Maximum, Maximum Principal Stress Trends





Stress is dramatically reduced by tabs.

FEA Results

- Solder Fatigue Life Trends (2mm δ)

$$N_f = \left(\frac{1.31636}{\Delta EQPS} \right)^{1.96078}$$

Fatigue Life (Cycles) for 0.2"/min Case						
	No Tab		0.1" Tab		0.2" Tab	
Tab Thickness (in)	No Underfill	With Underfill	@ Cap	@ PCB	@ Cap	@ PCB
N/A	3.32E+03	1.86E+05				
0.005			2.25E+10	1.15E+05	4.55E+14	8.83E+04
0.01			1.01E+09	1.34E+05	2.25E+13	8.31E+04
0.016			5.24E+05	3.27E+04	1.20E+10	3.33E+05
0.022			3.27E+04	1.95E+04	4.12E+06	1.13E+05

Tabs have similar fatigue life predictions to underfill case for solder.
Case without underfill is significantly less.

FEA Results

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- Copper Fatigue Life Trends (2mm δ)

Fatigue Life (Cycles) for 0.2"/min. Case		
Tab Thickness (in)	0.1" Tab	0.2" Tab
0.005	2.85E+07	7.18E+07
0.01	4.74E+06	4.53E+07
0.016	1.48E+06	1.18E+07
0.022	1.29E+06	4.78E+06

S-N Curve* of commercially pure (99.98%) Copper between interval of 10^4 and 10^7 and Grain Size of 70 μm

$$\sigma_a = k_1 N_f^{-b}$$
$$k_1 = 388MPa$$
$$b = 0.107$$

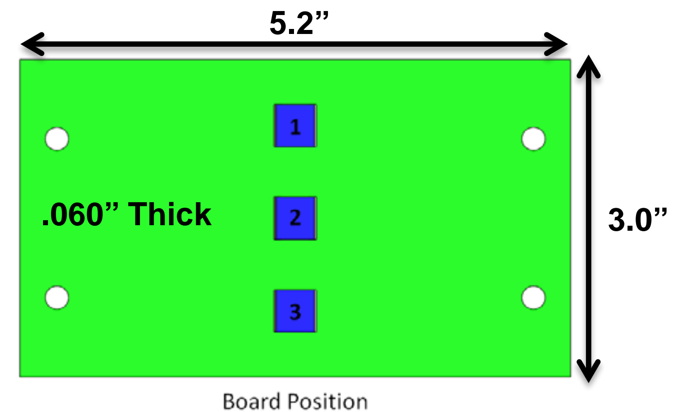
Fatigue life prediction for copper is higher than corresponding solder predictions.

* Lukáš, P. & Kunz, L. (1987). Effect of grain size on the high cycle fatigue behaviour of polycrystalline copper. *Mat. Sci. Eng.*, Vol. 85, pp. 67-75, ISSN 0023-5416.

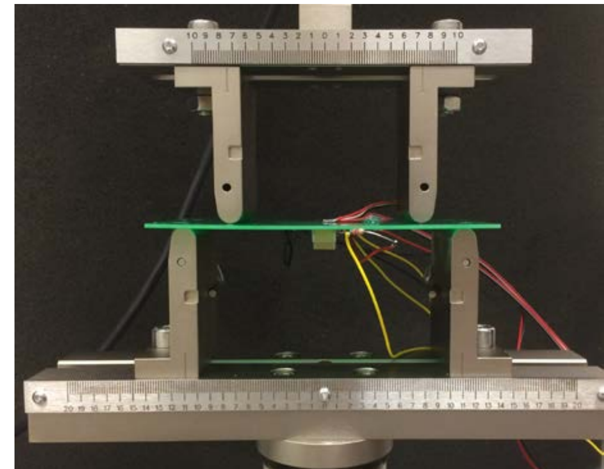
Lab Scale Testing - Setup

- Modified JESD22B113 – JEDEC Board Level Cyclic Bend Test Method
  - Novacap Capacitor (size 3640)
    - P/N RC3640R184K152PX250
  - 4 Point Bend Test w/ 75mm and 110mm spans
  - 12mm deflection (no cycling) @ 20”/min. deflection rate
    - Tests were repeated until failure occurred (or didn’t occur)
  - Strain/Capacitor voltage monitored during test to determine failure

Test Matrix			
Position	Board A	Board B	Board C
1	0.00	None	None
2	0.15	0.00	0.20
3	0.20	None	None

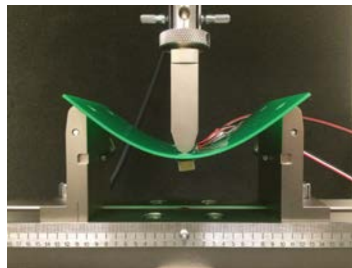


Board Position



Lab Scale Testing - Results

- Board A (Three Capacitors)
  - Failure of SMT Capacitor seen at 10 mm deflection on 1st bend – solder crack closed itself upon returning to initial state
  - Copper tab capacitors did not fail
- Board B (One SMT Capacitor)
  - Failure seen on 3rd test around 12 mm deflection (switched to 3 point bend test)
- Board C (One 0.200" Tabbed Capacitor)
  - Did not fail after 13 tests. Tried increasing the deflection on a 3 point bend test to 20mm and the capacitor still did not fail.



Board C @ 20mm deflection

Pre Test | Post Test

Board A

Board B

Board C

Capacitors with copper tabs performed better than the surface mount capacitor.

Conclusions / Path Forward

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- Thermal Deflection Study
  - FEA indicates that solder fatigue life is increased by including underfill and removing overcoat from capacitor. The opposite is also true, fatigue life is reduced by removing underfill and including an overcoat.
  - Experimental cross sections of samples that have been thermal cycled ~1500 times show large cracks/gaps in solder with overcoat.
- Copper Tab Mounting Study
  - ***Feasibility*** is confirmed by preliminary FEA and quasi-static, simple 4 point bend test
  - **More work is needed** to vet out all questions related to the method:
    - Better material model needed for copper in high strain-rate regime
    - Potted configuration needs to be analyzed in dynamic and thermal environments
    - Dynamic verification testing needs to be performed
    - Need to look at different tab geometries/materials