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NDIA National Defense Industrial Association

58th Annual Fuze Conference
July 7 – 9, 2015

A Synchronous Addressed Communications Method for Coordinating Multiple Outputs and Effects in Fuzing Systems

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Abstract and Problem Statement

- Problem Definition
  - Selectable yield warheads require multiple effects
  - Multiple Effects useful in Multiple-layer penetration weapons
  - Robust and simple means to set multiple firing modules are required
    - Reduces manufacturing costs
    - Lowers number of conductors of cables & size of connectors
- Excelitas proposes a multi-drop network system to set multiple effects
- This presentation will cover
  - The elements used in the proposed communication interface
  - An explanation of how the elements interact
  - The work to date on the development of the interface
  - The path forward toward interface development

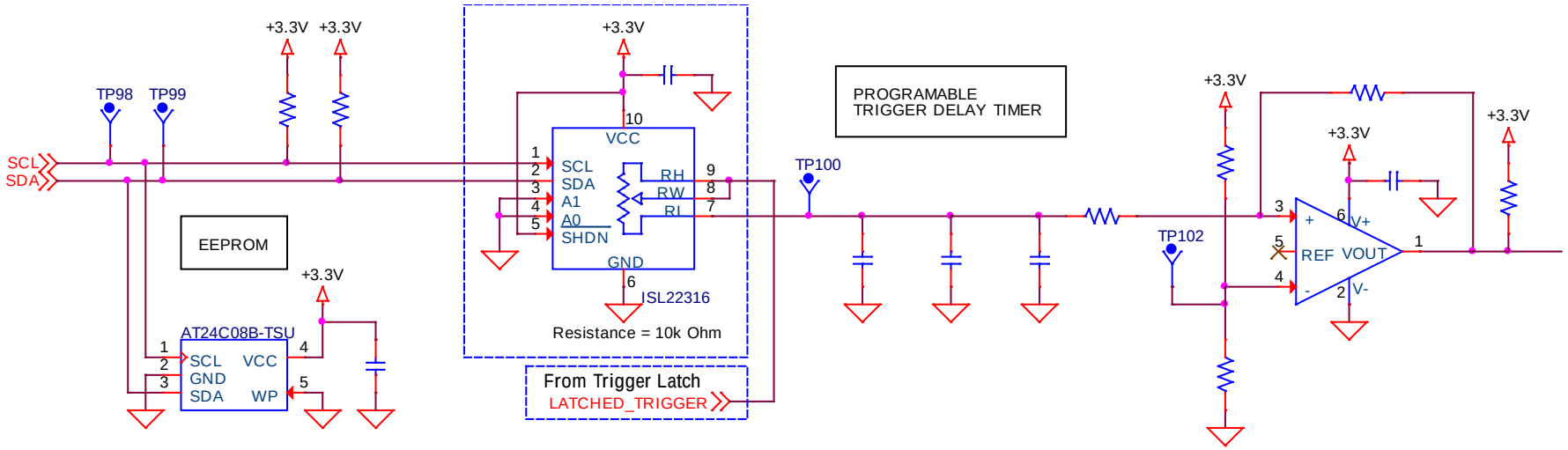
Developing a Solution

- Motivation for the effort
  - Originally motivated in response to NAC (National Armaments Consortium) research topic FUZ-15-27
    - Requested development of low voltage power and communication protocols for selectable yield, multi-mode, and multi-purpose warheads
  - The solution needs to be compliant with Fuze industry standards
    - MIL-STD-1901A for Ignition Safety Devices (ISD)
    - MIL-STD-1316 for Electronic Safe and Arm Devices (ESAD)
- The proposed system integrates commercially available networking systems with a robust 4-wire networking system
  - The solution should allow the operation of an internal data bus
  - Should also have a Electronic Module (EM) to multiple Firing Module (FM) interface that will be robust in a missile environment
    - Selected ARINC-429 physical layer interface
      - ARINC (Aeronautical Radio Incorporated)
        - Tutorial from Avionics Interface Technologies: http://aviftech.com/files/2213/6387/8354/ARINC429_Tutorial.pdf

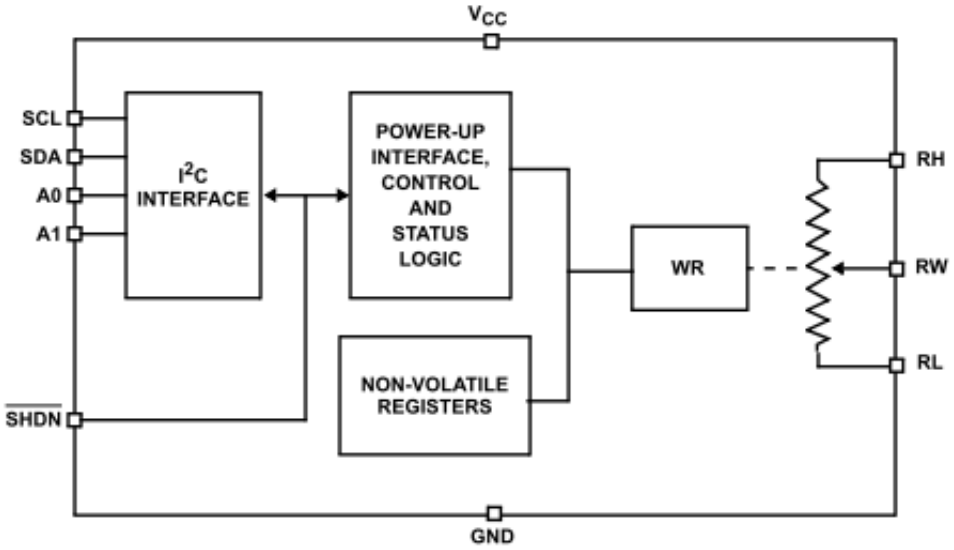
I²C as the FM Internal Bus

- The I²C (Inter-Integrated Bus) is a multiple-master, multiple-slave bus introduced by Philips (now NXP) in 1982
  - Originally developed to allow microprocessor control of electronics through slave peripheral devices
  - Widely adopted as a standard by the electronics industry
- I²C is used in a wide variety of peripheral components useful to the defense industry
  - Digital Potentiometer
  - Non-volatile Memory (EEPROM, Flash, etc.)
  - Data acquisition
    - Analog to Digital Converter (A/D)
    - Digital to Analog Converter (D/A)
    - Temperature Sensors
    - Digital Output Accelerometer
  - Port Extension

Example of I²C use in Fuzing



- I²C Components used in Fuzing
  - Digital Potentiometer
    - Calibration
    - Analog Timer (as above)
  - Data Acquisition
    - Time, temperature, acceleration
  - Mux and Switches
  - Non-volatile Memory



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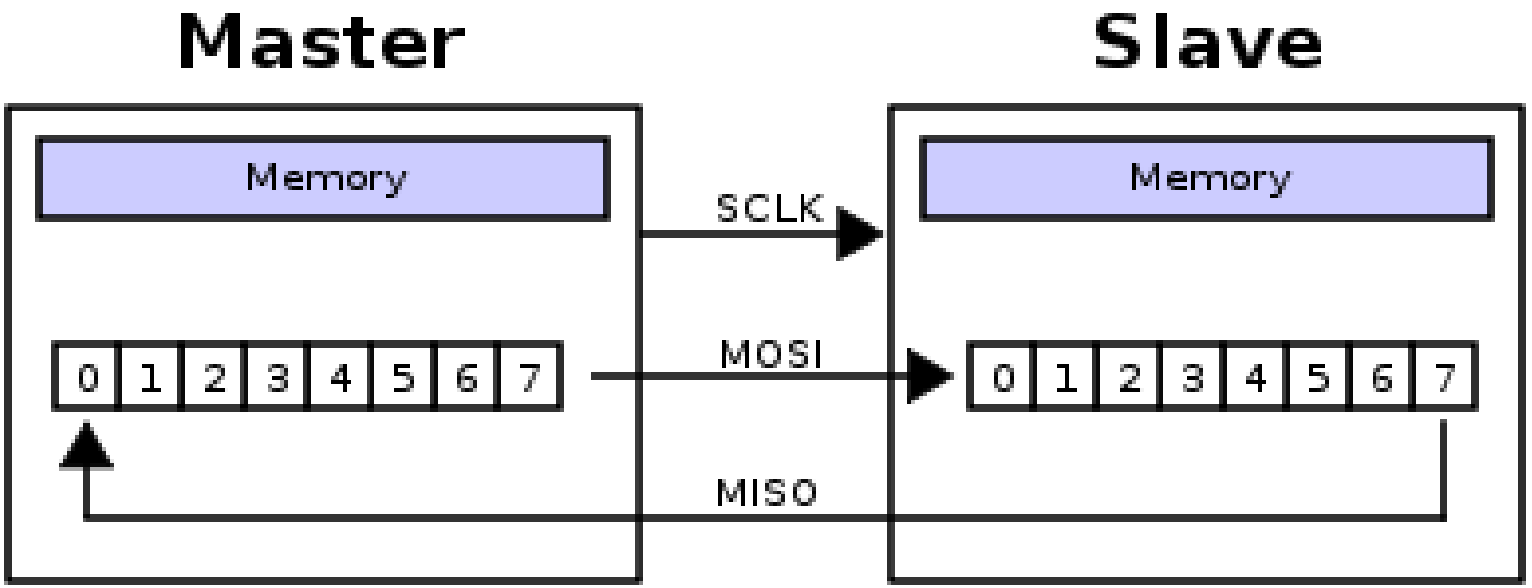
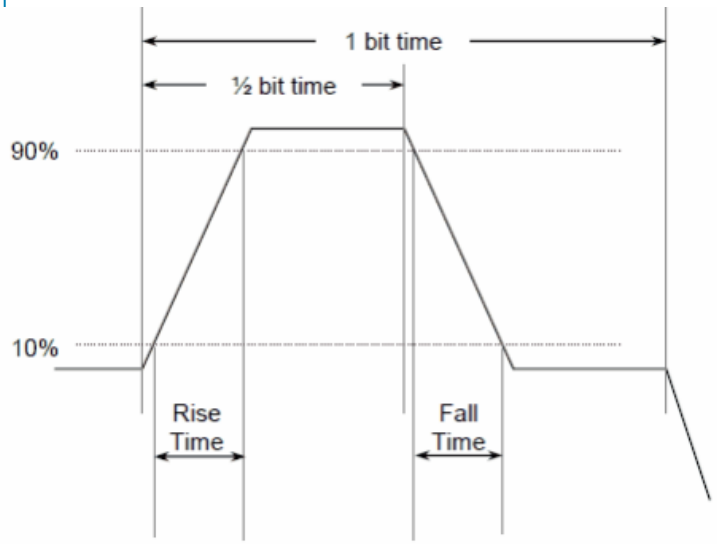
Serial Peripheral Interface

- SPI (Serial Peripheral Interface) is a synchronous full-duplex bus developed by Motorola Semiconductor (now spun off as Freescale)
  - Data is exchanged through a circular buffer
  - De facto standard available on microcontrollers and programmable logic
- Bus is designed to have one master and one slave per control line
  - Used for External Memory and LCD I/O
  - Common interface for Data Acquisition components (A/D, D/A)

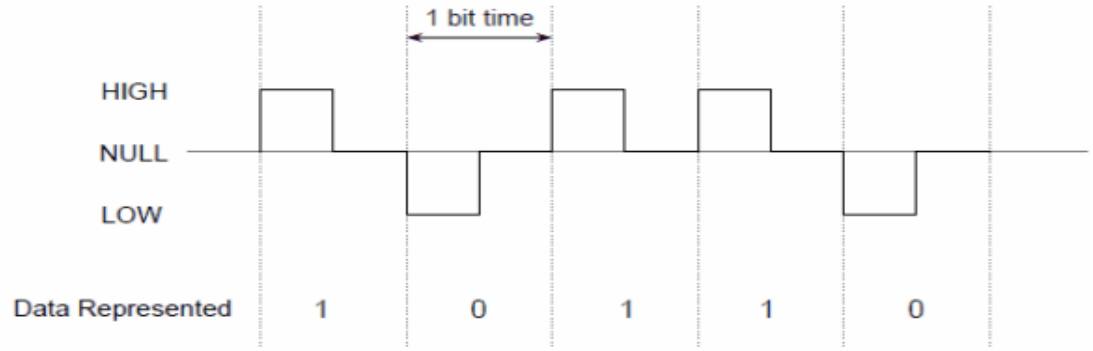


ARINC 429 Data Bus Between Modules

- ARINC-429 is a combination of a two-wire full-duplex physical layer and communication protocol
- Physical layer consists of one line transmitter and one or more receivers
- 100KHz bit rate proposed
  - Four bit separation between data frames
  - Tri-state signal combining signal and clock
  - Clock integrated through 50% duty cycle between data and ground state



ARINC429 Signal Waveform Parameters



ARINC429 Signal Encoding

	High Speed
Bit Rate	100 kbps ± 1%
1 bit time	10 µsec ± 2.5%
½ bit time	5 µsec ± 5%
Rise Time	1.5 µsec ± 0.5 µsec
Fall Time	1.5 µsec ± 0.5 µsec

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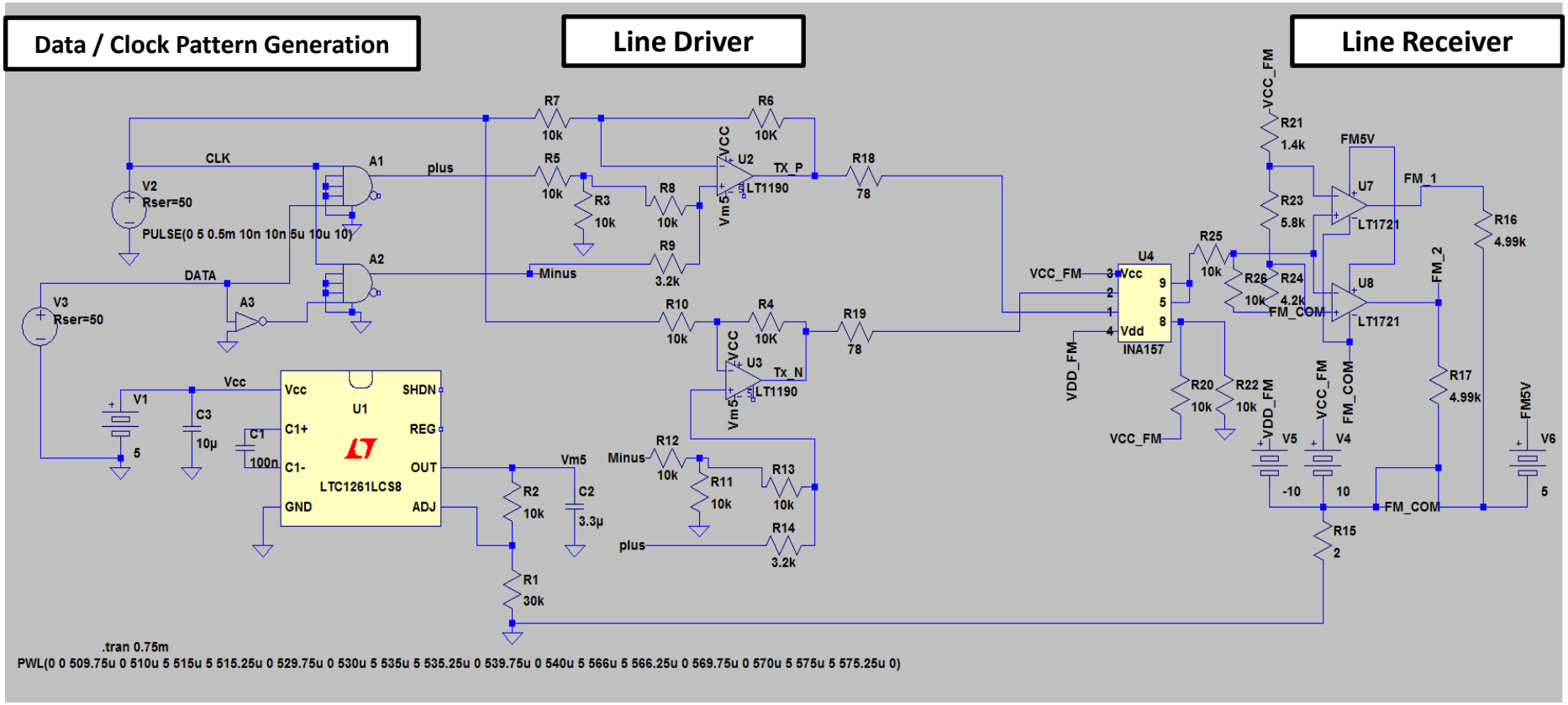
ARINC 429 Protocol Tutorial. Avionics Interface Technologies, pp. 10-11

Physical Layer Simulation with LTSpice



- First Step was an electrical simulation of a single line driver and receiver
  - Simulation performed using LTSpice®
  - Models from Linear Technology and Texas Instruments
- Return impedance simulated by separation of 2Ω between driver and receiver

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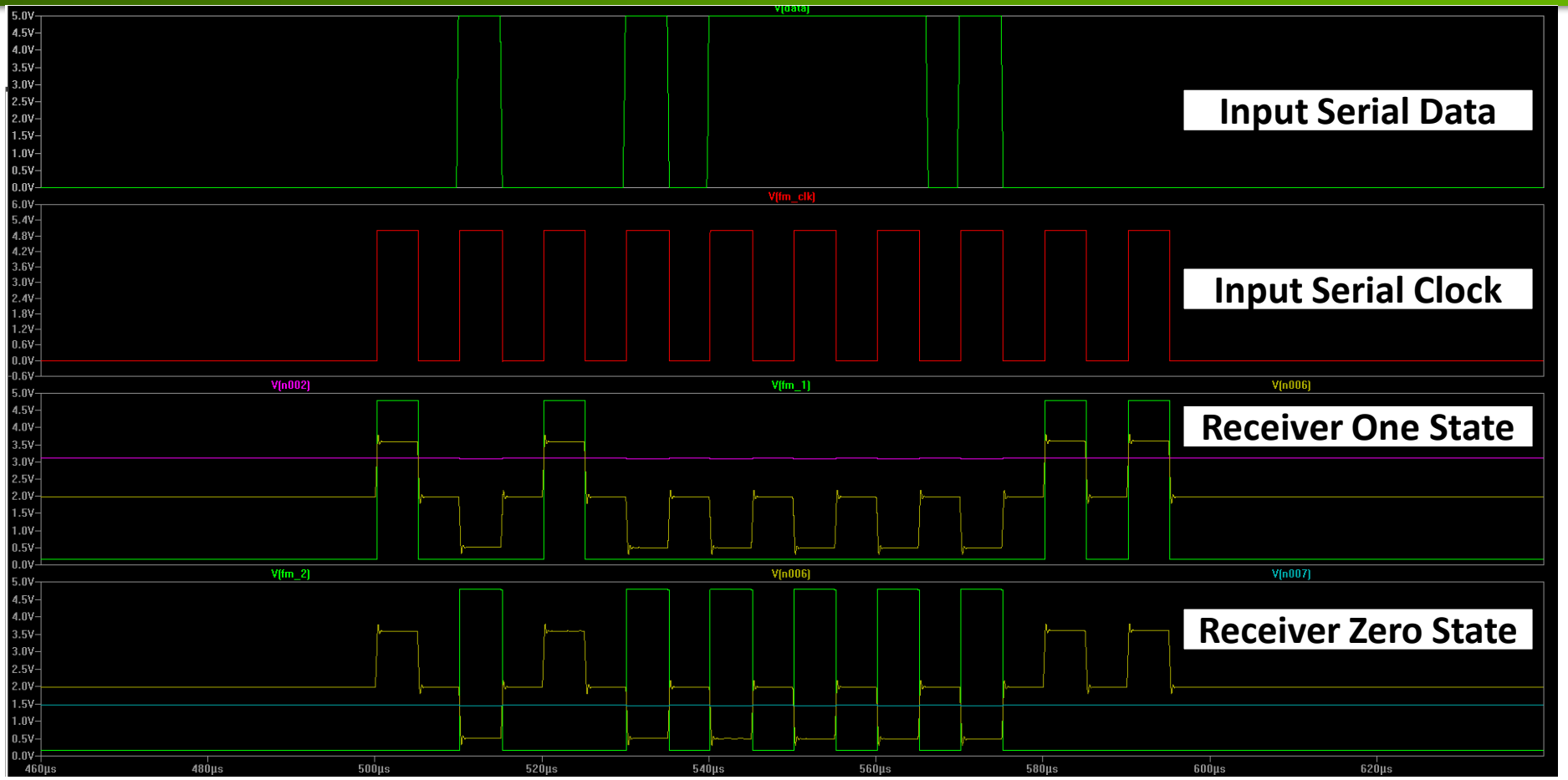
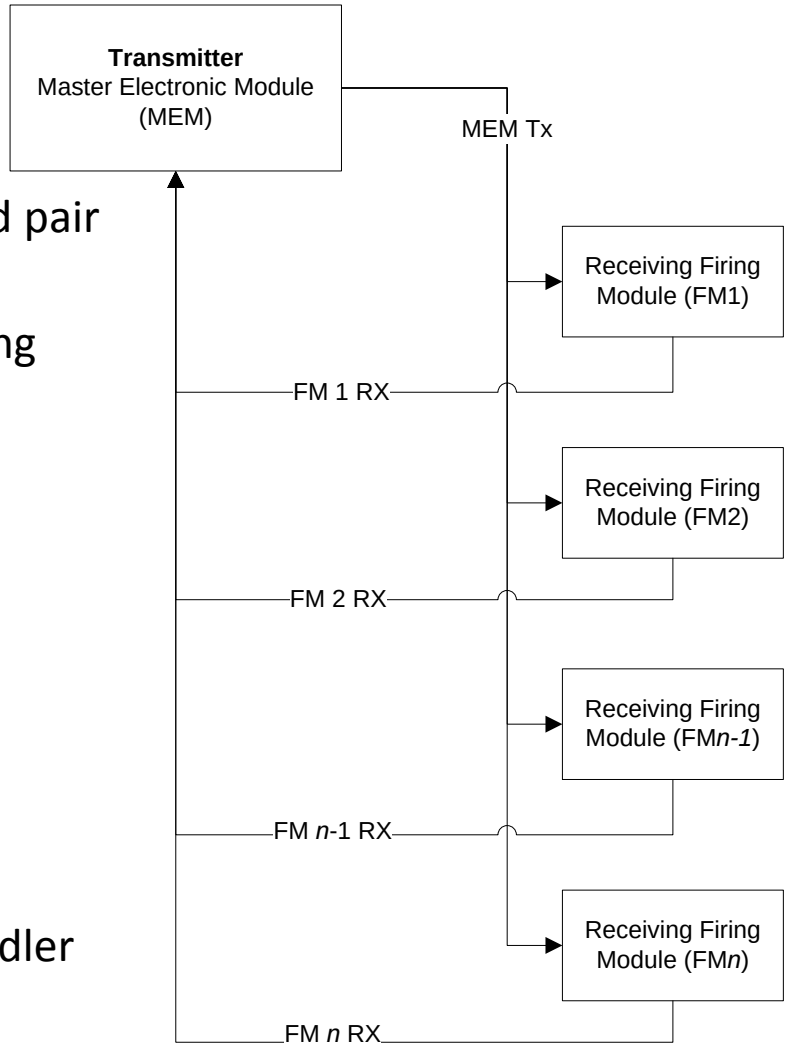
Line Driver and Receiver Simulation Plot



- Line Driver and Receiver Transient Plot
  - Signal in Yellow is Output of Differential Amplifier U4
  - Digital state outputs from comparators U7 & U8 using signal from U4

Network Structure

- Prototype Network Structure
  - Full-Duplex four-wire structure between Electronic Module and Firing Modules
    - Physically connected with shielded twisted pair cable
    - Separate pair for transmission and receiving channel
  - MEM – Master Electronic Module
    - Originates Communications requests
  - Up to *n* Firing Modules (FM)
    - Respond to requests
    - "Speak only when spoken to"
    - Only one FM Line driver active
      - All others in High impedance output mode
  - FM address handling through a protocol handler
  - Prototyped with programmable logic
  - ASIC envisioned for production use



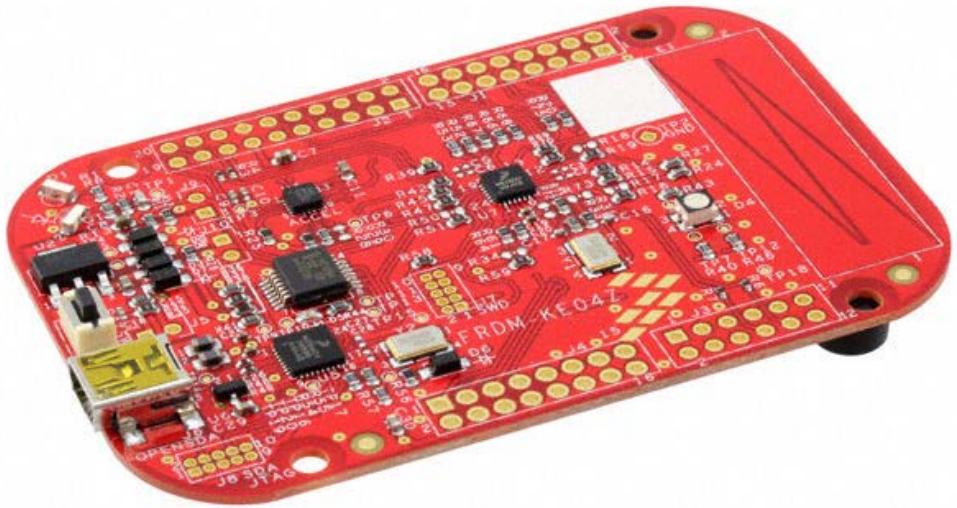
Network Frame Characteristics

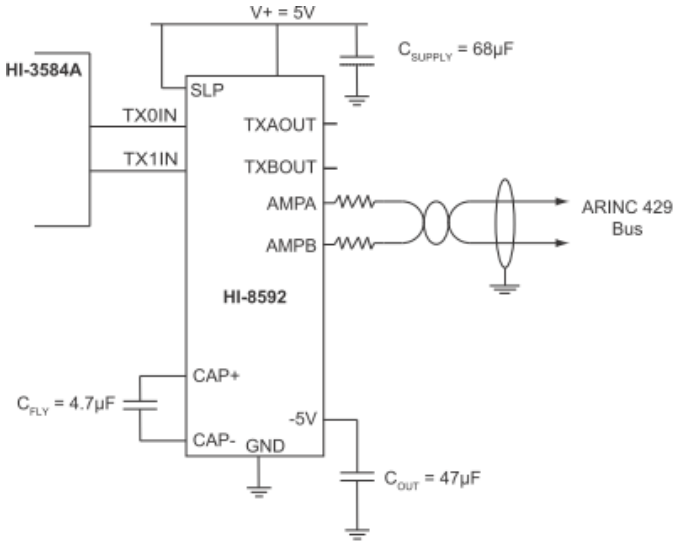
32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
P	EF	OF	#Frame			Frame Data																R/W		FM Address							

- The data frame shall be 32 bits long
- The general elements of the frame consists of:
  - FM Address
    - Eight bits (255 FMs and Electronic Module)
  - Write or Read
    - 0 for Write, 1 for read
  - Frame data – 16 bit length
  - Frames in transaction (1 to 8)
  - First Frame (OF) and End Frame (EF) bits
    - Beginning and ending of a transaction
  - Parity bit
    - Insures that that number of 1s transmitted is an odd number
    - Bit set or cleared to obtain count

Component Selection

- Initial proof of concept will incorporate elements of the FM Mockup
  - Digital Potentiometer to simulate Analog Timer
  - Digital Switch to handle timing range selection
- Initial proof of concept of FM protocol handler performed with a Kinetis® microcontroller board
  - Standard Arduino R3 form factor for expansion board design
  - Single SPI and I^2C ports on board target device
- Off the shelf Line Driver and Receiver (Holt Integrated Circuits HI-8592)





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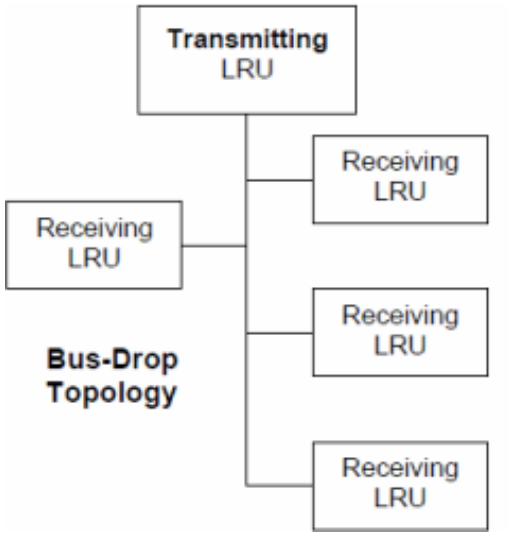
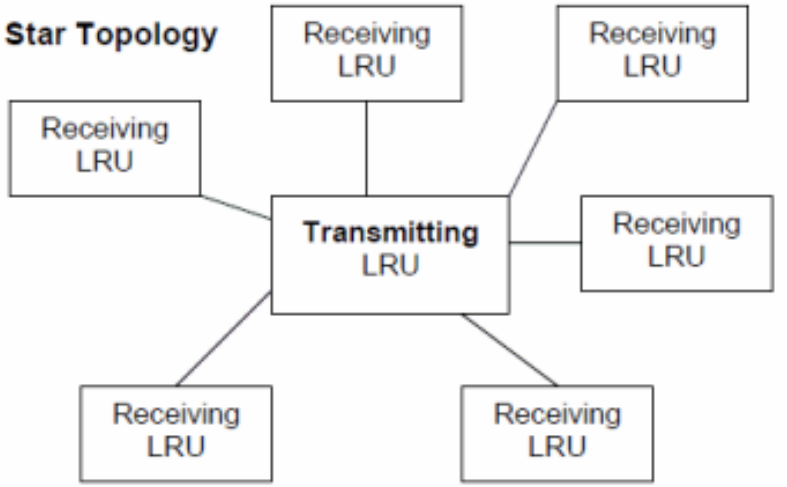
The Path Forward

- Design Validation of Proof of Concept
  - Will modify a small ESAD design to prototype MEM and FM modules
    - ESAD successfully tested in high acceleration missions
- Design will prove and "dial in" network use in *n*-FM system
  - Examine reliability of strict Bus Drop versus Star Topology
- Network part of larger effort in multi-effects Fuze system development
  - Contact transmission, Charging, and Low Voltage Power Supply
- Goal of a cost-effective, highly manufacturable multi-effects Fuze





ARINC 429 Protocol Tutorial. Avionics Interface Technologies, pp. 6

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