Office of the Secretary of Defense
National Aeronautics and Space Administration

"An Evaluation of Flash Cells Used in Critical Applications"

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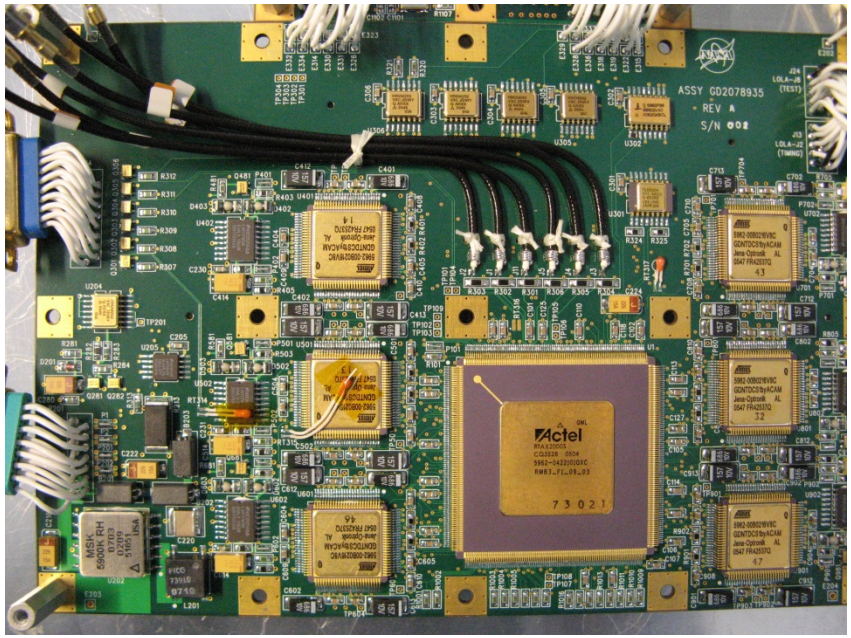

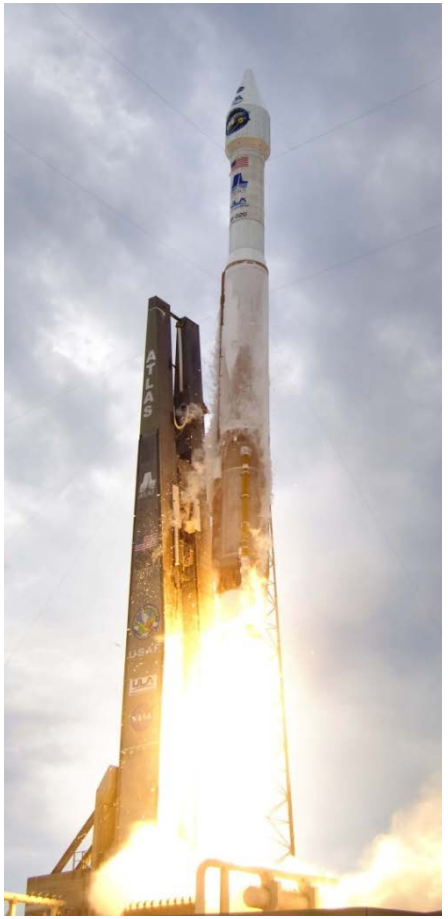

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Experiment Goals

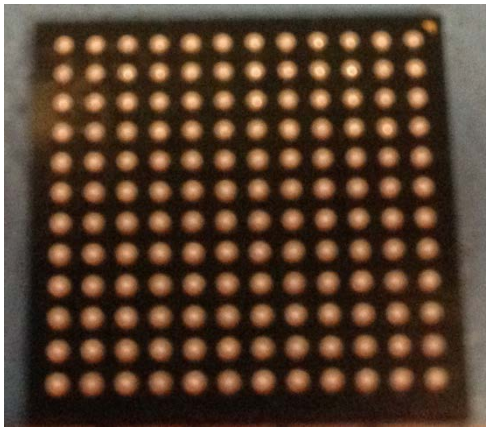
- **The primary objective is to determine the probability of extrinsic flash cells in the population and to determine how that will limit the device's lifetime.**

- **A secondary objective is to track the intrinsic populations lifetime which is a function of storage temperature.**

- **A third objective is to measure the flash cells' susceptibility to other environmental stresses.**
  - Electromagnetic (EM) radiation
  - Neutron irradiation
  - Electrostatic Discharge (ESD)
  - Heavy Ion Irradiation (total dose tests have been conducted)
  - Other (please suggest)

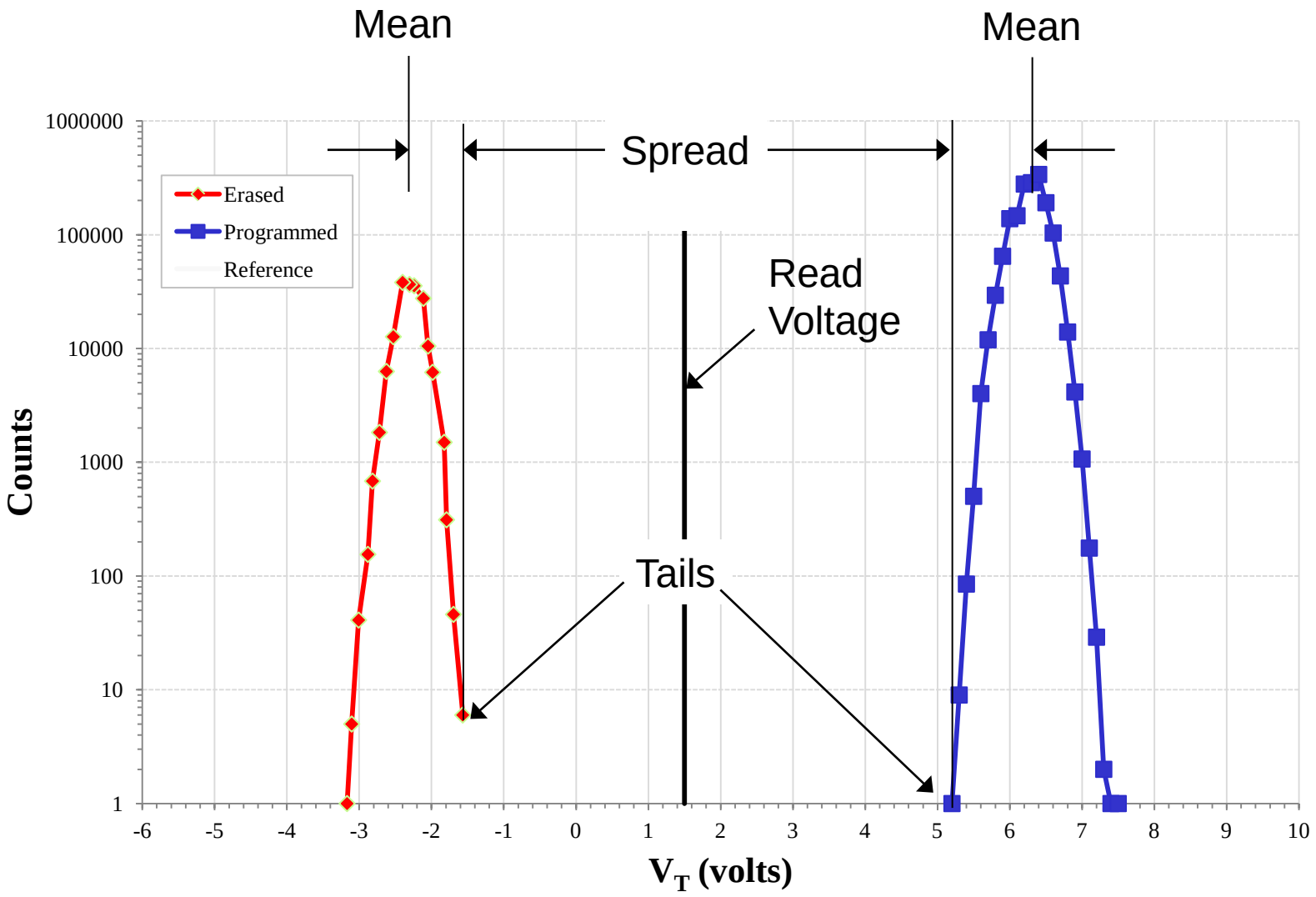
Description of DUTs

- **Microsemi (Actel) A3P250L FPGA**
  - Relatively small FPGA
  - PBGA (Plastic Ball Grid Array) Package (FG144)
  - Single Foundry for all DUTs
  - Most parts from one wafer lot (QLWY8)
    - Small number of DUTs from a second wafer lot (QLG10)



- **9 Logic Designs Used**
  - No artificial test structures
  - Logic blocks designed by different authors and styles (including macro generators)
- **10 Erase-Program-Verify Cycles for Each Device**
  - Realistic stress for our applications.
  - Manufacturer’s rating: 500 cycles
- **Complements and Extends work by Sandia National Labs**
  - Sandia is a Department of Energy organization that has previously investigated flash cell reliability. See references at the end of this presentation.

Population Analysis: Metrics

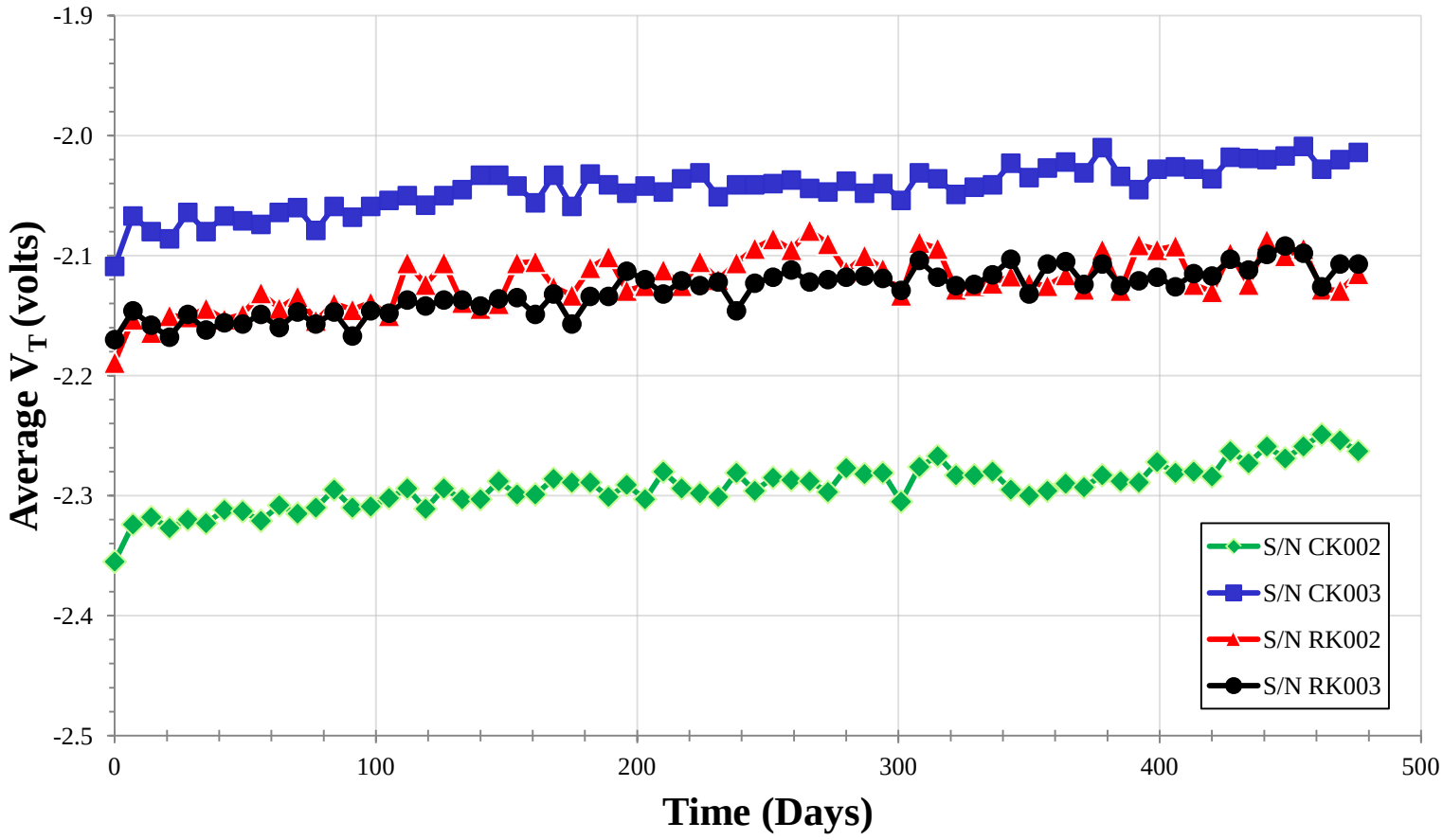


Initial Effects

- Engineering tests and data in literature showed an initial rapid movement in threshold voltage after configuring a device
- Three devices configured and then margin tested once per day
- Protocol updated: Baseline margin tests after several weeks of “settling time”

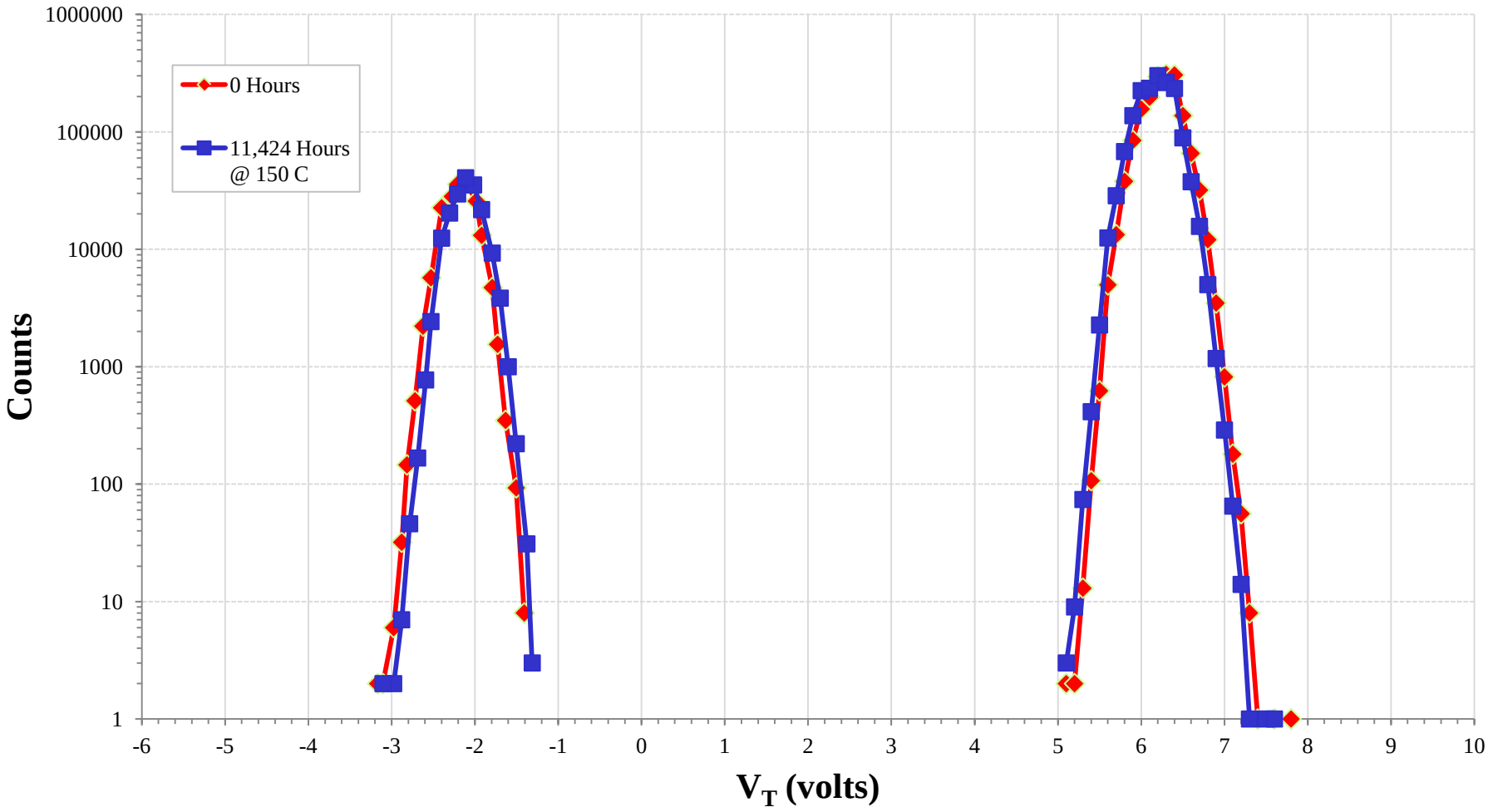
Erased: Engineering Run

A3P250L FPGA Average Erased V_T
11,424 Hours @ 150 °C, March 26, 2016

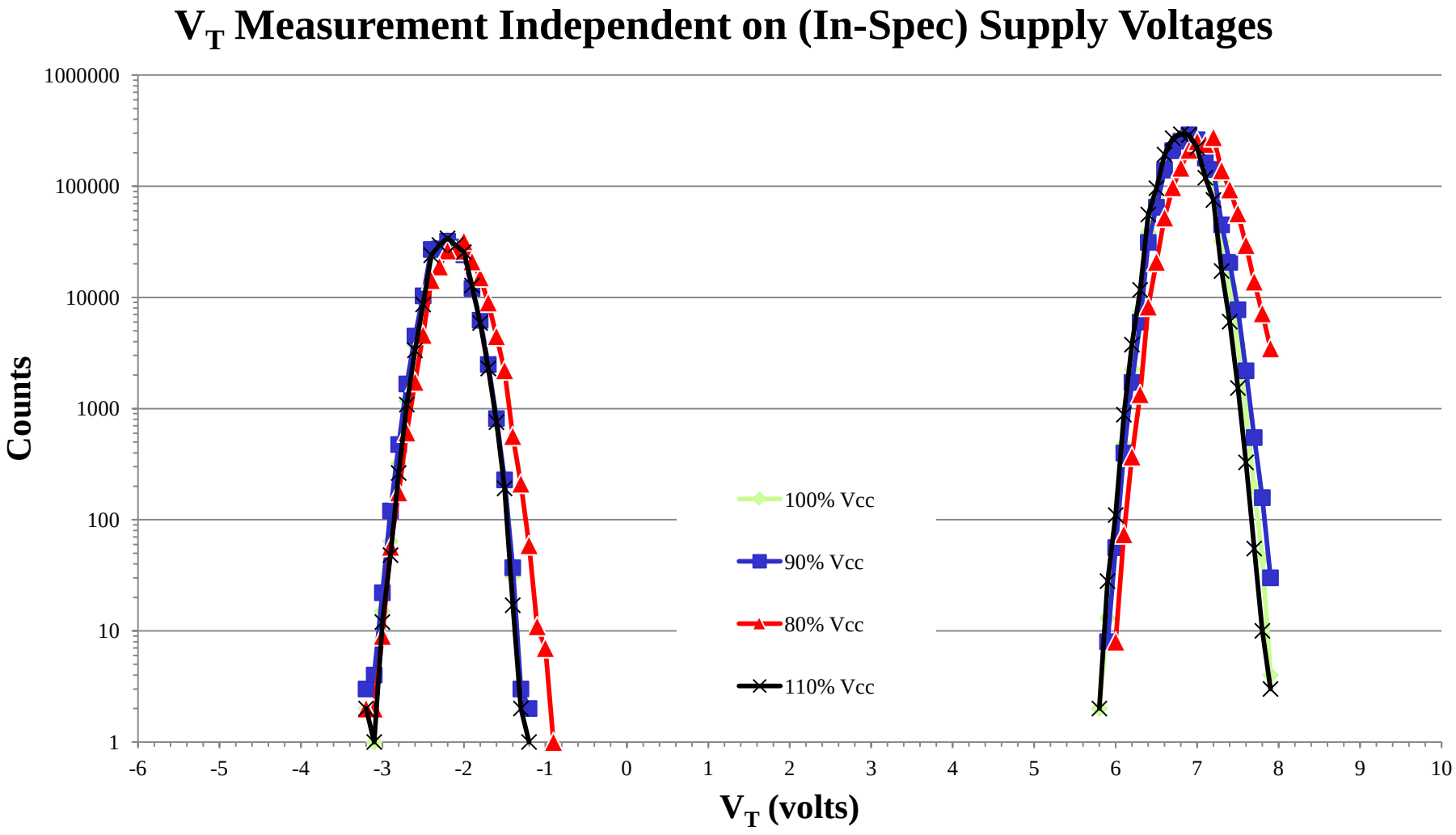


Effects of 150 °C Bake on Flash-based FPGA

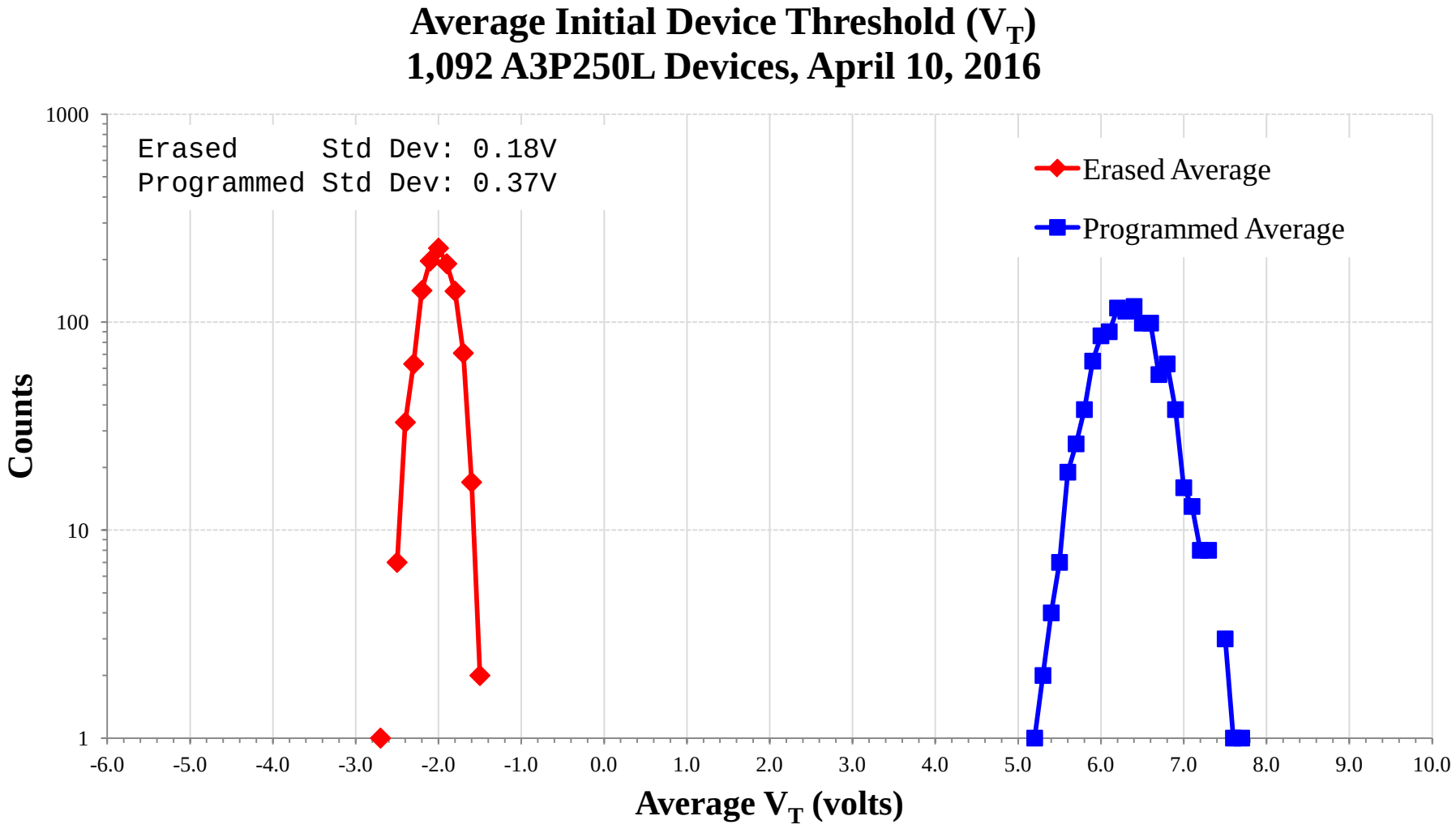
V_T Delta After 11,424 Hours @ 150 °C: S/N RK003



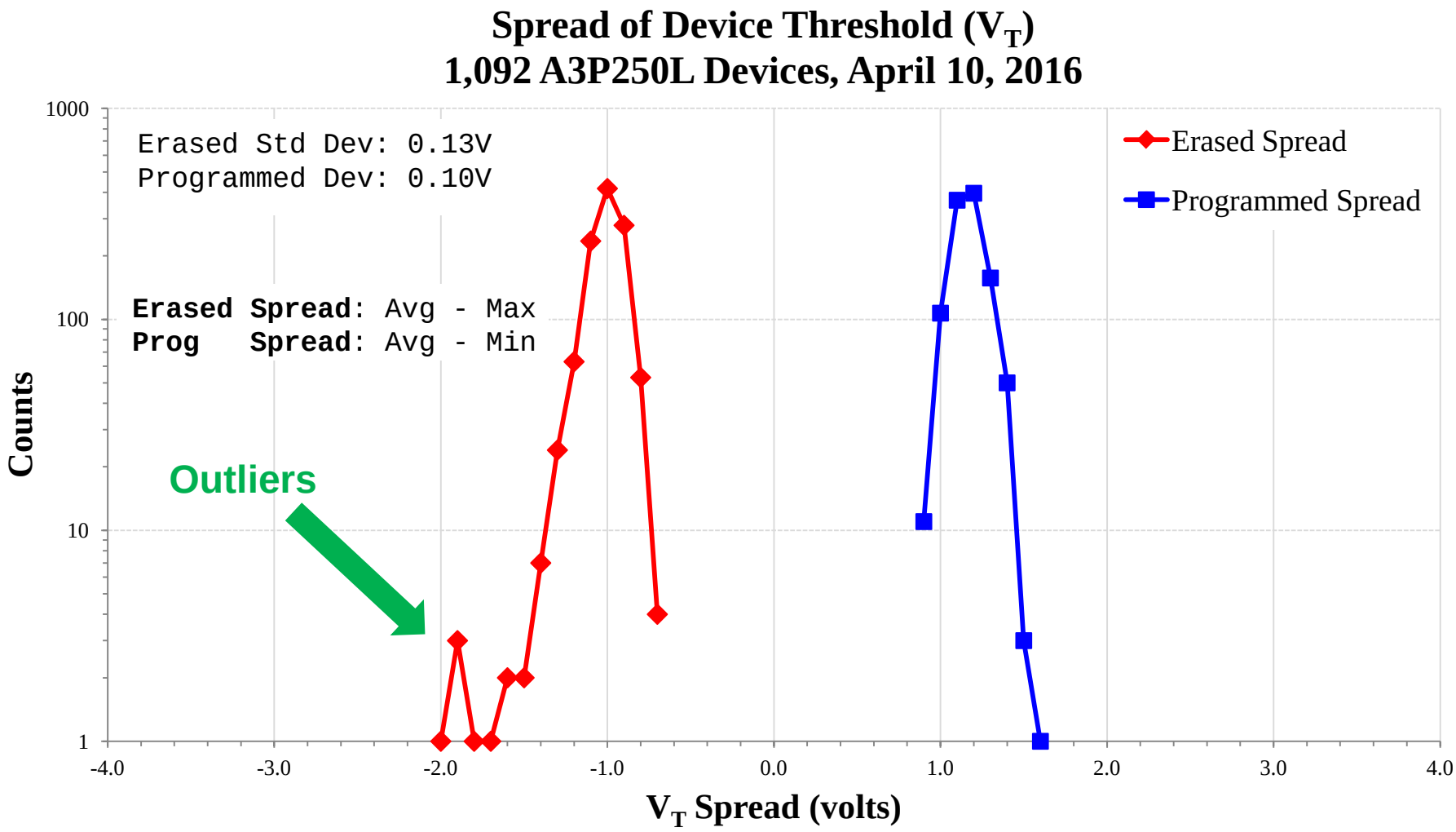
Instrumentation Sensitivity



Population Analysis: Mean

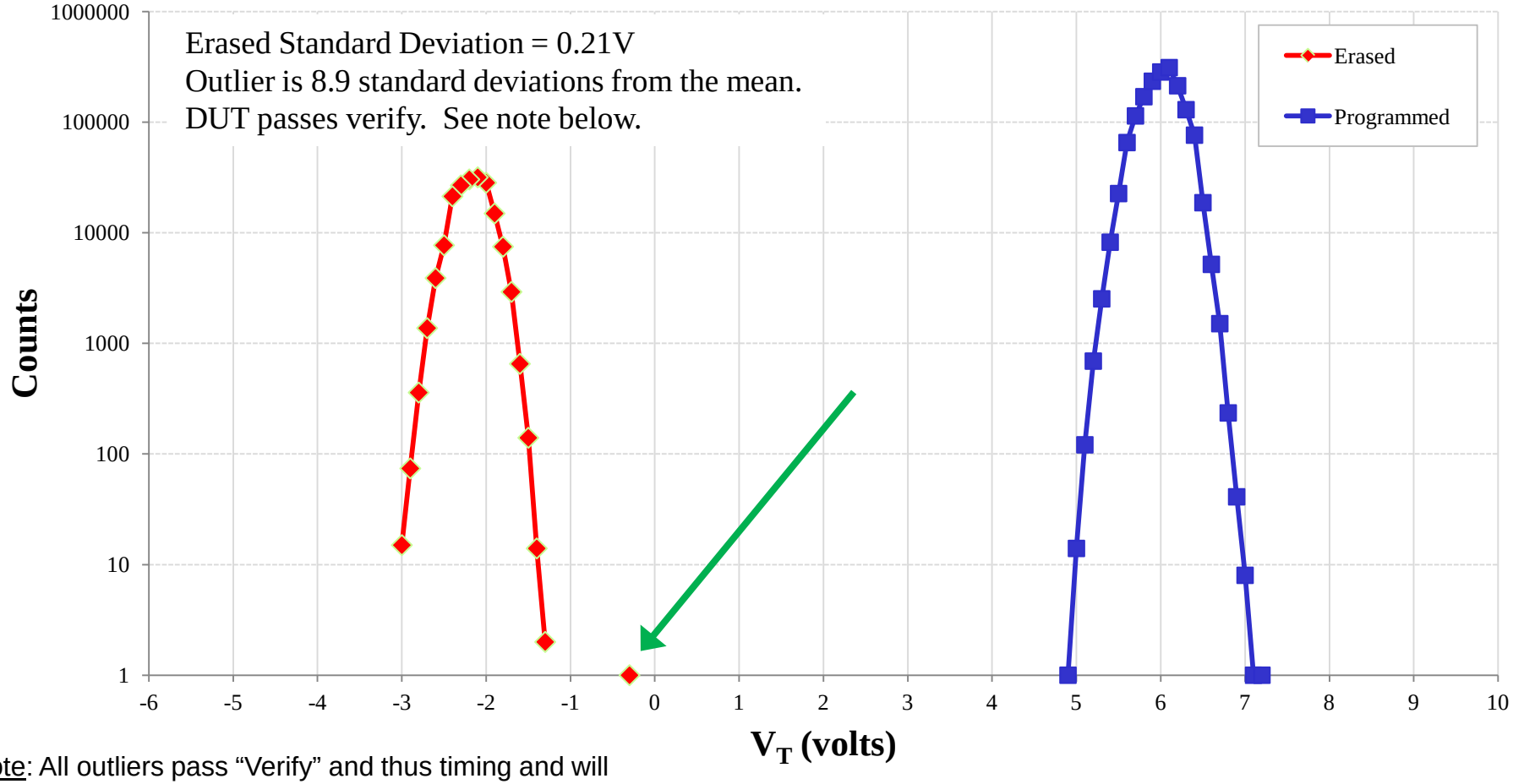


Population Analysis: Spread



Population Analysis: Outlier

S/N F0205, Initial Margin Test, March 10, 2016

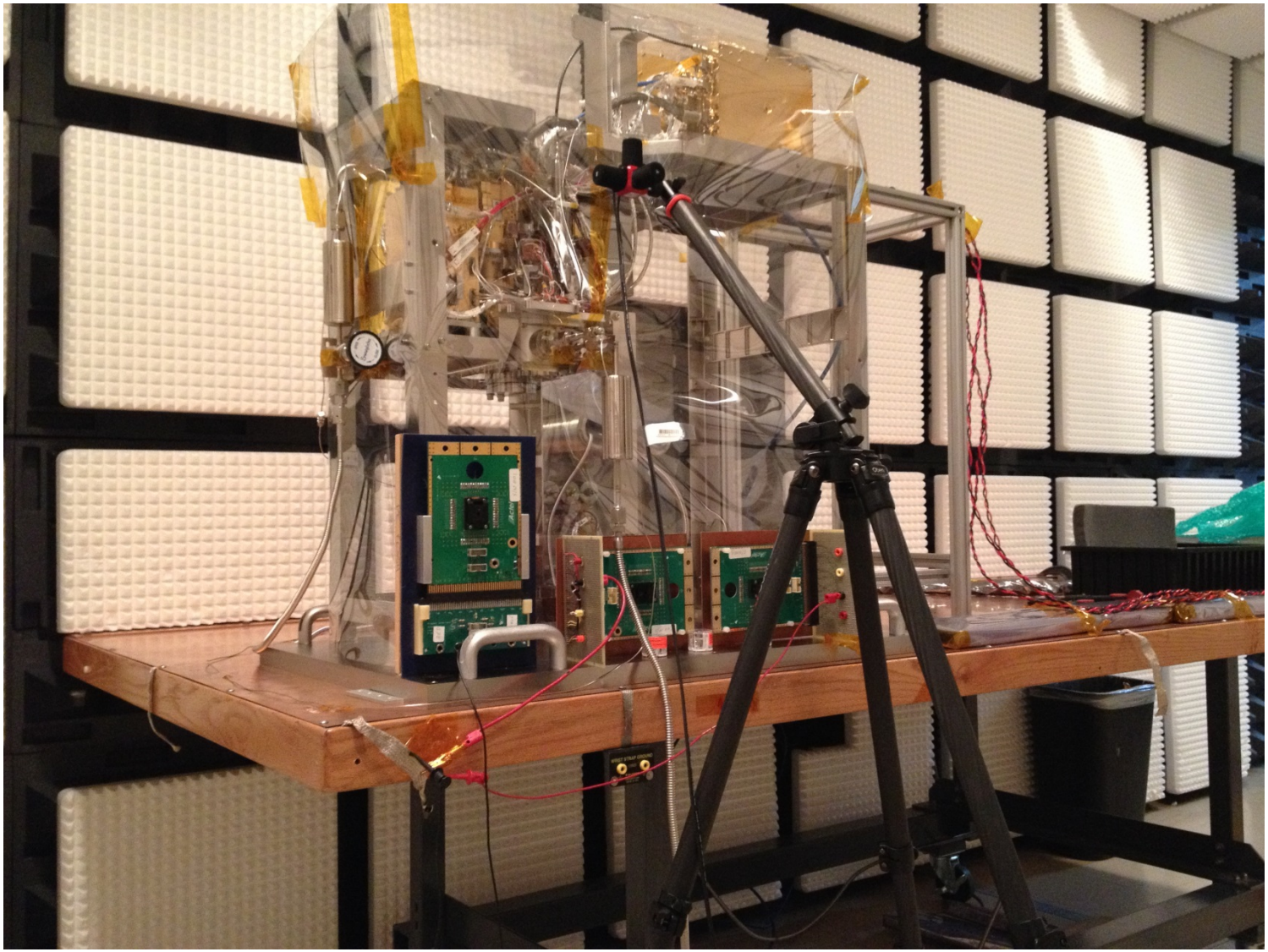


Note: All outliers pass "Verify" and thus timing and will be tracked over three temperatures to verify reliability.

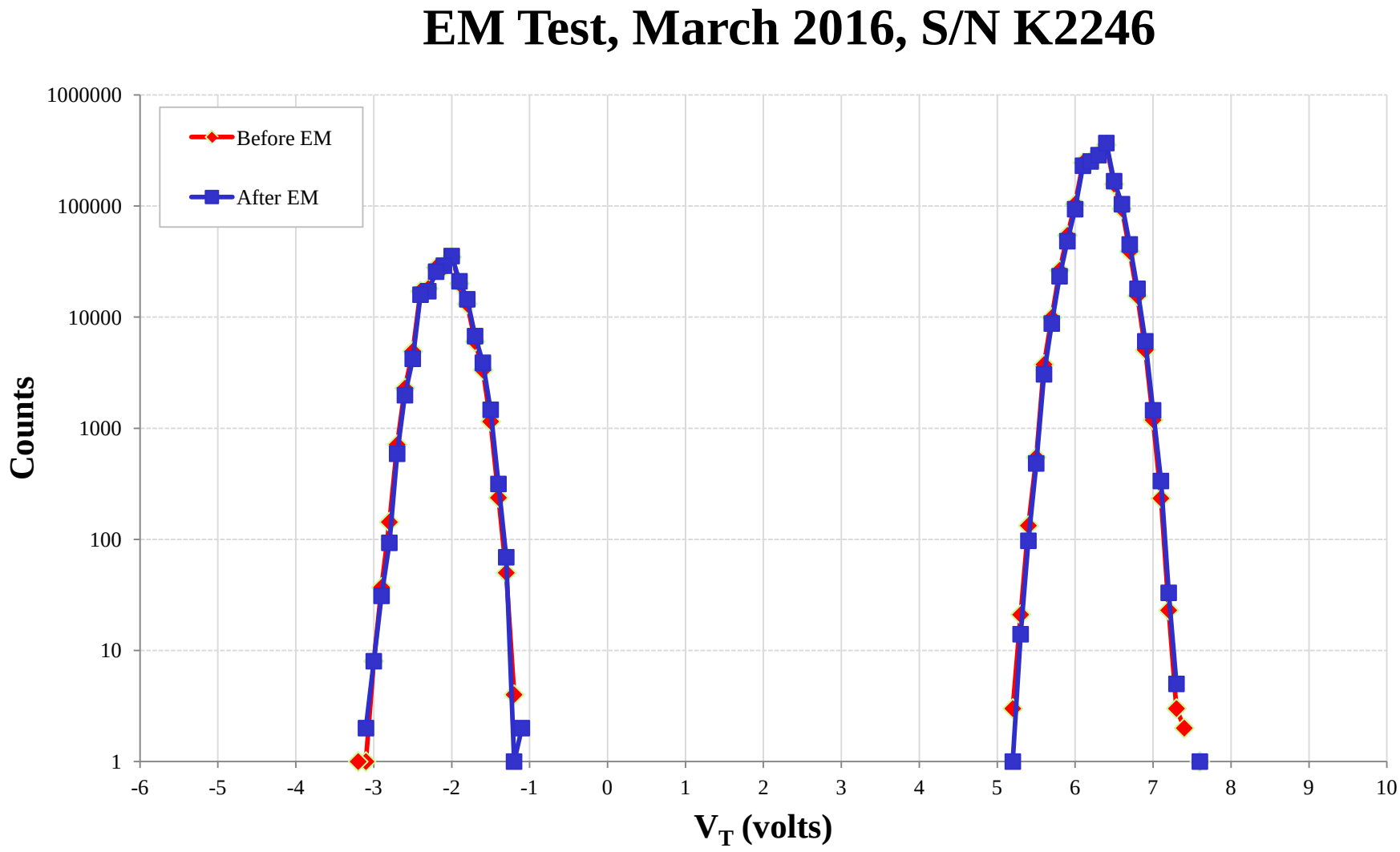
EM Susceptibility: Introduction

- **Goal: Determine Susceptibility of Flash Cell to EM Radiation**
- **DUT Configuration:**
  - 3 DUTs
  - Unpowered
  - No enclosure or other shielding
  - Simple Board: Traces for power, ground, and programming (not I/O)
- **A first test: Tested with a NASA Mars science instrument**
  - Multiple Runs with horizontal and vertical polarizations
  - Test levels based on science instrument (not fuze) requirements

EM Susceptibility Testing Facility

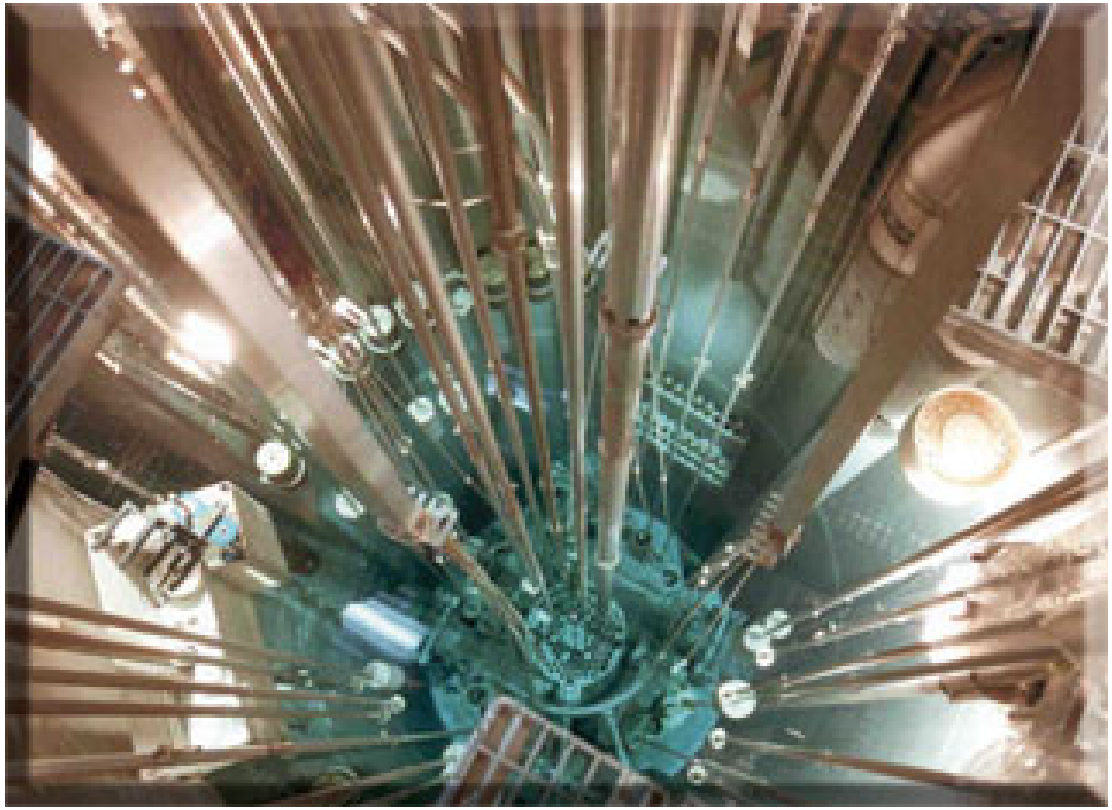


EM Susceptibility Results (typical)



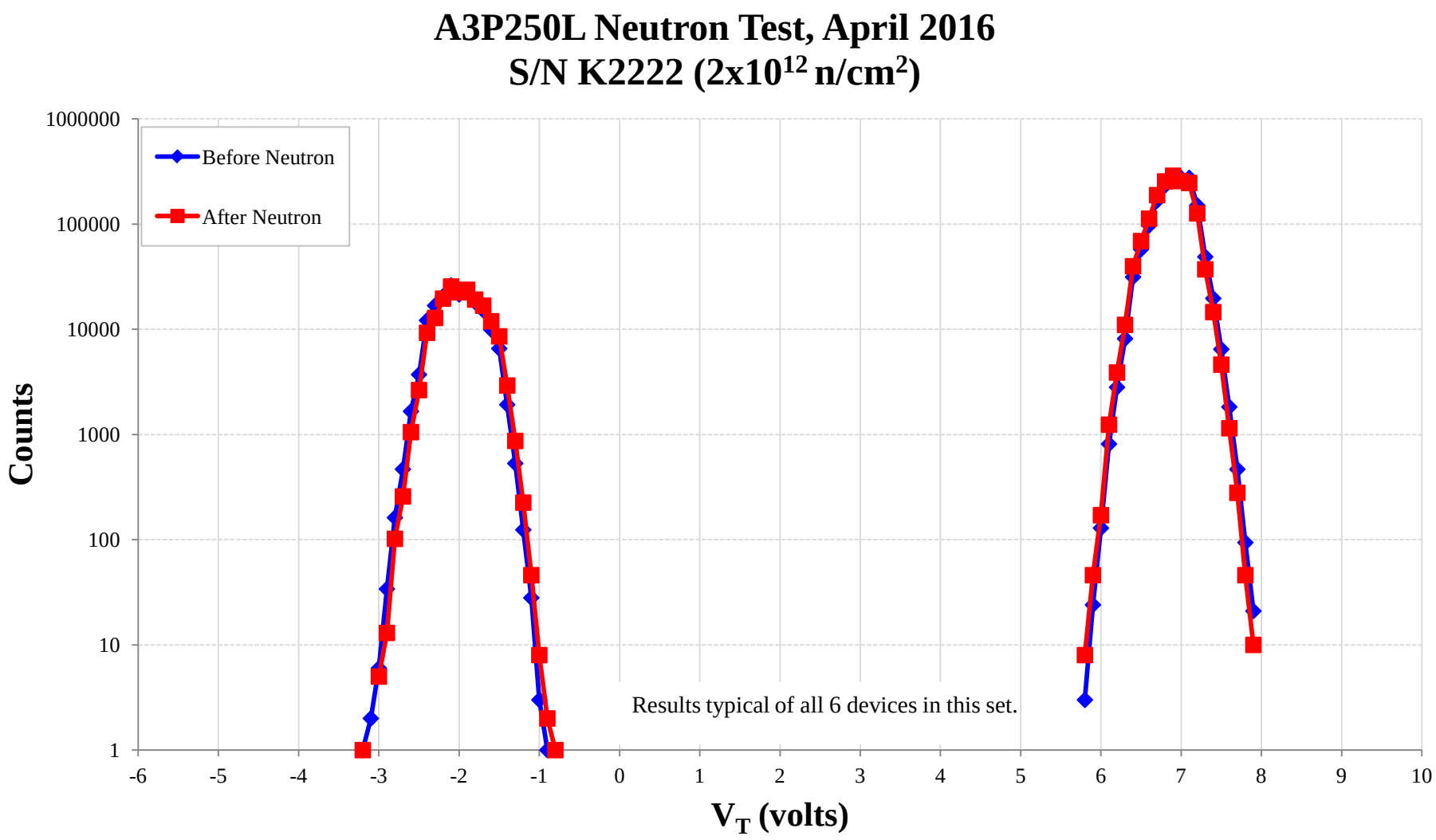
Neutron Susceptibility Testing

- **Sample Size:** 20 DUTs
- **Test Levels:**
  - 2 x 10^{12} n/cm^2 (7 DUTs)
  - 2 x 10^{13} n/cm^2 (7 DUTs)
  - 2 x 10^{14} n/cm^2 (6 DUTs)
- **Test Conditions**
  - 1 MeV equivalent spectrum
  - DUTs unbiased
  - DUTs' balls shorted
- **Test Facility:** McClellan Nuclear Research Center (near DMEA)

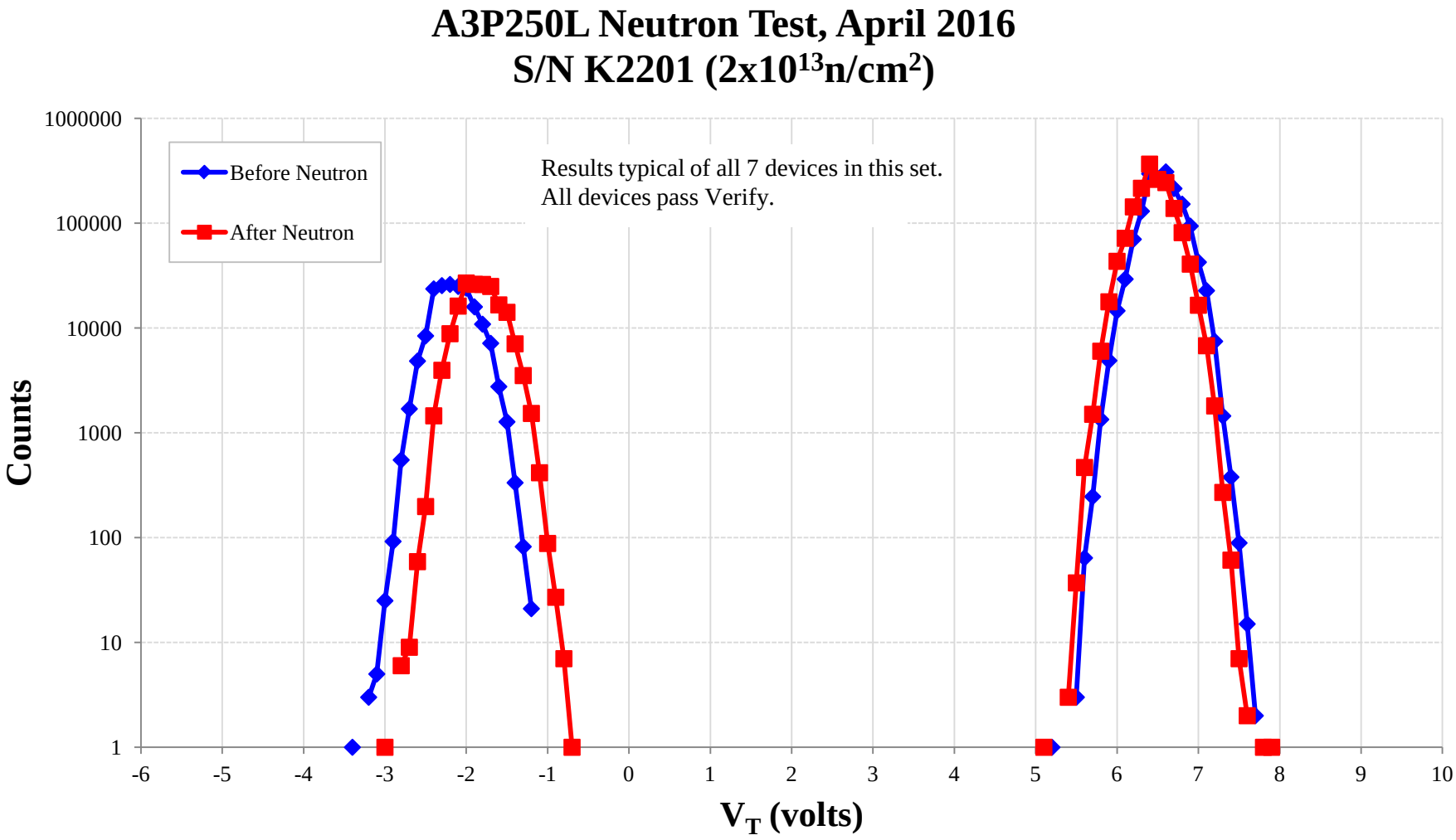


MNRC Reactor in Operation

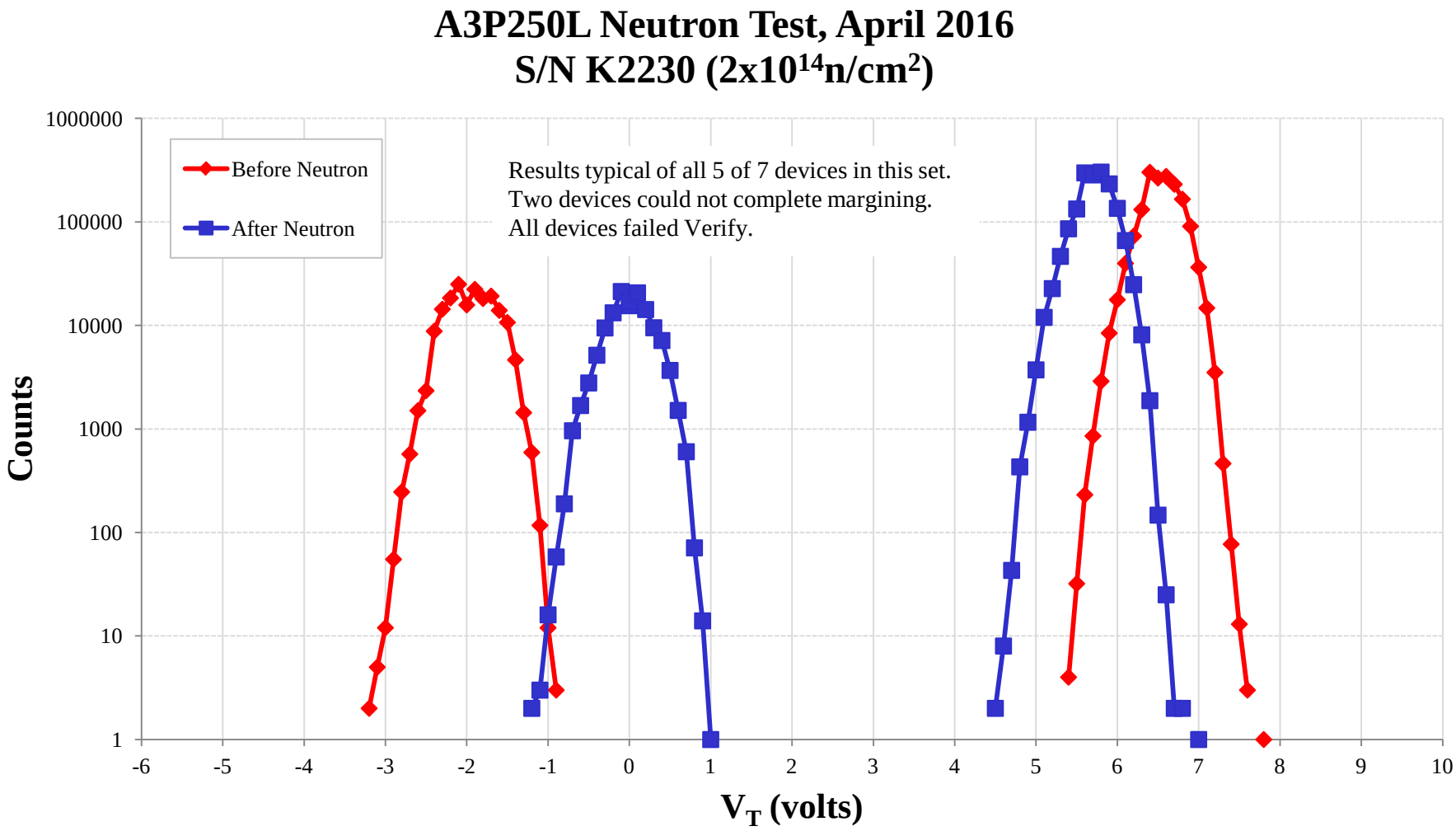
Neutron Testing: 2 x 10^{12} n/cm^2



Neutron Testing: 2 x 10^{13} n/cm^2



Neutron Testing: 2 x 10^{14} n/cm^2



ESD Susceptibility Testing

- **Sample Size:** 20 DUTs
- **Test Levels:**
  - Phase Lock Loop (PLL): 500V
  - Other Power and I/O: 2 kV
- **Test Equipment:** Thermo Scientific MK.1 ESD and Static Latch-up Test System
- **Results**: DUT card fabricated and tests designed. Test system is down and will be repaired.

Temperature Experiment Summary

Engineering Run

- 4 devices at 150 °C for 11,592 hours + 2 control samples
- One failure at 11,592 hours; probably mechanical, part undergoing analysis
- V_T shift very small

Large Population

- # of Parts Programmed: 1,091
- # of Parts Margined: 1,091
- # of Outliers[1]: 7 (~0.6%)
- # of Part Failures[2]: 1

322 Parts Soaking at 150 °C
327 Parts Soaking at 125 °C
333 Parts Soaking at 25 °C (add'l 57 being prepared)

[1]All outliers were erased cells and passed Verify test.
[2]K1631 would not margin or verify; likely non-flash failure, under failure analysis. All other DUTs passed.

Summary, Conclusion, and Path Forward

- **Test Method and Data Analysis Tool Development**
  - Utilize Device's Design for Test Capability
  - Write Semi-custom Data Analysis Tools
  - Produce Credible, Useful Results
- **Testing Large Populations Necessary**
  - Significant Variability Between DUTs
  - Detect Outliers (~ 0.6 % for the subject device)
  - Significant Difference in Device Retention Time
- **Investigate Tighter Threshold Voltage (V_T) Limits on Verify Operation**
- **Assistance Needed on EM Test Limits, Protocols, and Facilities**
- **Possible Future Large Population Test: TI Microcontroller**
- **Track Large Populations:**
  - Temperature Testing Ongoing (+25 °C, +125 °C, and +150 °C)
  - Outliers pass "Verify" and thus timing and will be tracked to verify reliability. Outliers are in each of the temperature groups.

References

- "**Anatomy of an in-flight anomaly: investigation of proton-induced SEE test results for stacked IBM DRAMs**," K. A. LaBel; P. W. Marshall; J. L. Barth; R. B. Katz; R. A. Reed; H. W. Leidecker; H. S. Kim; C. J. Marshall, IEEE Transactions on Nuclear Science, 1998, Vol.: 45, Issue: 6, pp. 2898 - 2903

- "**Long Term Data Retention of Flash Cells Used in Critical Applications**," K. Bergevin, R. Katz, and D. Flowers," 58th Annual Fuze Conference, July 7-9, 2015, Baltimore, MD.

- "**Viability of New COTS Technologies in Future Weapon Systems**," J.Marchiondo, et. al, Sandia National Labs, September 2010.

- "**Threshold voltage distribution in MLC NAND flash memory: characterization, analysis, and modeling**," Cai, Yu; Haratsch, Erich; Mutlu, Onur; and Mai, Ken, Proceedings of the Conference on design, automation and test in europe, ISSN 1530-1591, 03/2013, DATE '13, pp. 1285 – 1290.

- **"High Reliability FPGAs in Fuze and Fuze Safety Applications**," O'Neill, K., 59th Annual NDIA Fuze Conference, May 3-6, 2016, Charleston, South Carolina.