High Reliability FPGAs in Fuze and Fuze Safety Applications

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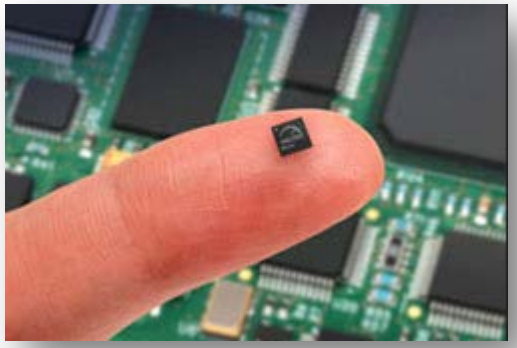
Agenda

- Why use FPGAs in Fuze applications
- Antifuse FPGAs in Fuze and Fuze safety systems
  - Heritage and Outlook
- Flash FPGAs – considerations for Fuze Safety and Arming
  - Architecture and Programming
  - Reliability, Retention, Qualification
  - Radiation
  - Power consumption
  - Heritage and Outlook
- Conclusion

Why FPGAs in Fuze and Safety Applications

- Many reasons to use FPGAs for integration of logic circuits in fuze safety and arming systems
  - Cost effective
    - No non-recurring engineering cost, unlike custom circuits (ASICs)
  - High levels of integration
    - Fuze safety and arming circuits can easily be integrated into modern FPGAs
  - Small form factor
    - Flat pack and fine ball grid array packages
  - High reliability
    - Millions of units shipped, extensive reliability data, various screening levels
  - Low power consumption
    - For battery-powered equipment, or thermally-constrained environments



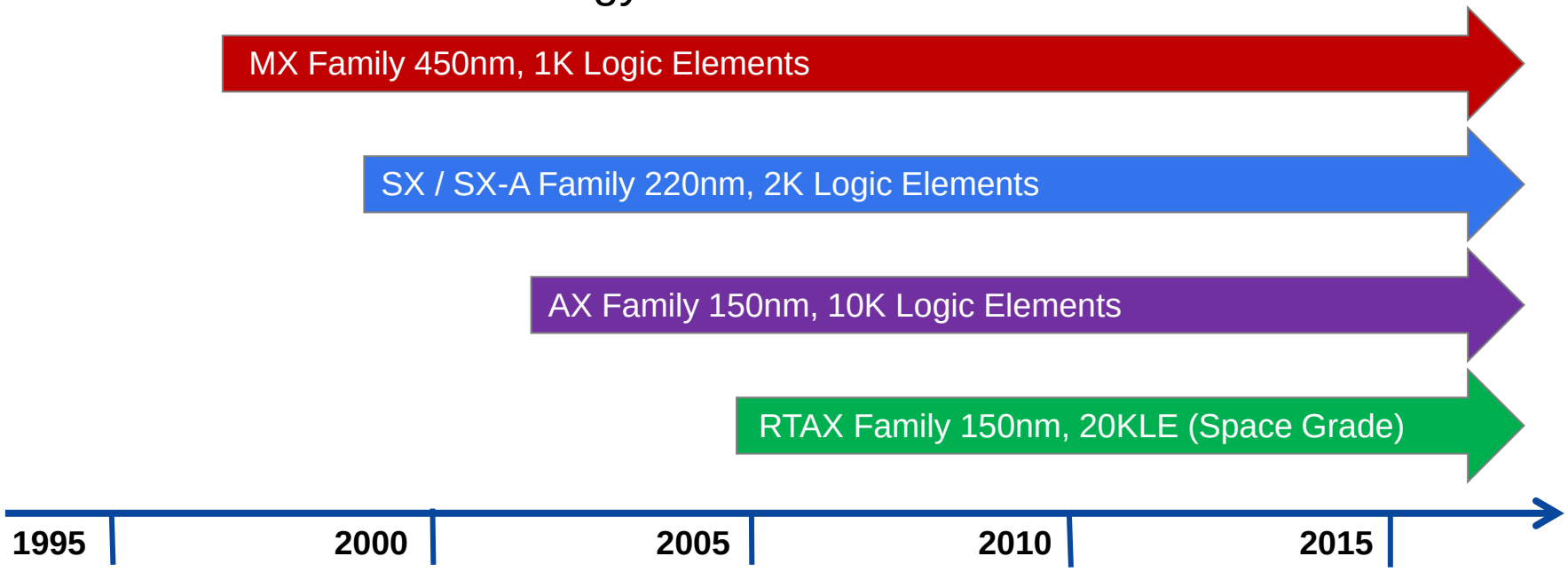
3mm x 3mm CS81 Package

Antifuse FPGAs in Fuze applications

- Microsemi antifuse FPGAs have a long heritage in fuze applications

Antifuse FPGA Outlook

- Microsemi has a policy of long term production
  - We hold many years of wafer stock after fab production has ended
  - 12 month last time buy, plus 6 month shipment window after final order
- No new antifuse technology introduction since 150nm in 2002



Now is the time to start thinking about Flash FPGA technology for next generation fuze safety and arming systems

Flash FPGAs
Considerations for Fuze Safety and Arming

Introduction to Flash FPGAs

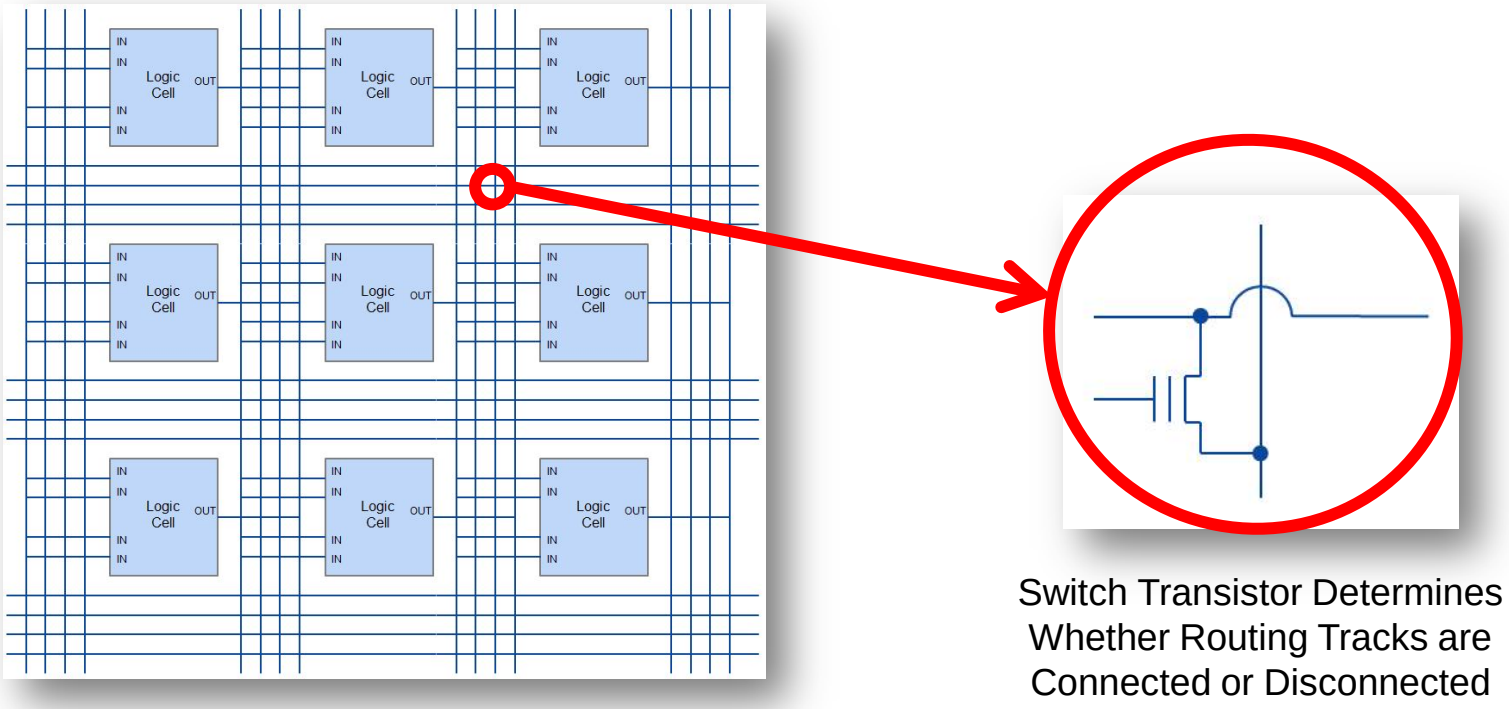
- Microsemi has a 20 year legacy in Flash FPGAs
  - ProASIC 0.25um
  - ProASIC Plus 0.22um
  - ProASIC3 and derivatives 130nm
    - Igloo (low power FPGA), Fusion (FPGA + mixed signal), SmartFusion (FPGA + embedded MCU)
  - Igloo2, SmartFusion2 (FPGA + embedded MCU) 65nm
  - Next generation in development

- This presentation focuses on reliability studies and qualification data for the 130nm and 65nm Flash FPGA product lines
  - Current generation, 65nm (Igloo2, SmartFusion2)
  - Preceding generation, 130nm (ProASIC3, Igloo, Fusion, SmartFusion)

- Flash FPGA qualification heritage
  - ProASIC Plus (0.22u) qualified to MIL-STD-883B in 2005
  - ProASIC3 (130nm) was qualified to MIL-STD-883B in 2010
  - ProASIC3 (130nm) was qualified to QML class Q in 2015
  - Igloo2 and SmartFusion2 (65nm) were qualified to JEDEC JESD22 in 2013

Architectural Overview of Flash FPGAs

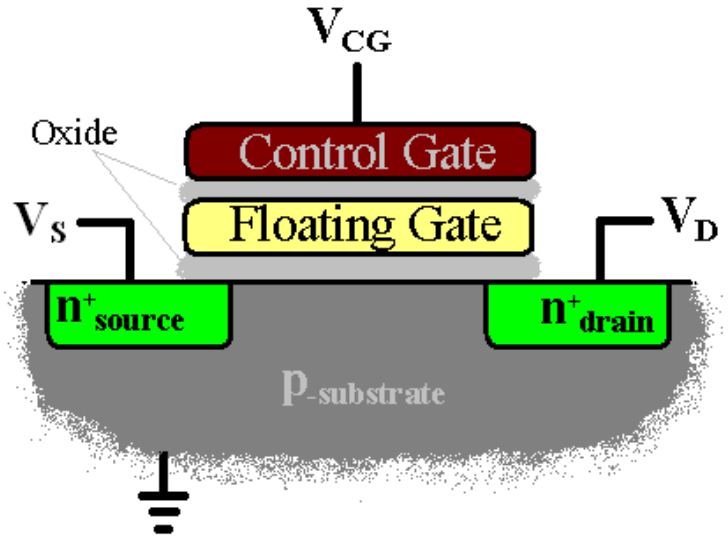
- All generations of Microsemi terrestrial Flash FPGAs have similar interconnect architecture
  - Device personality is determined by the connection of routing tracks
  - Switch transistor with floating gate connects or disconnects routing tracks
  - Non-volatile floating gate determines state of switch transistor – on or off

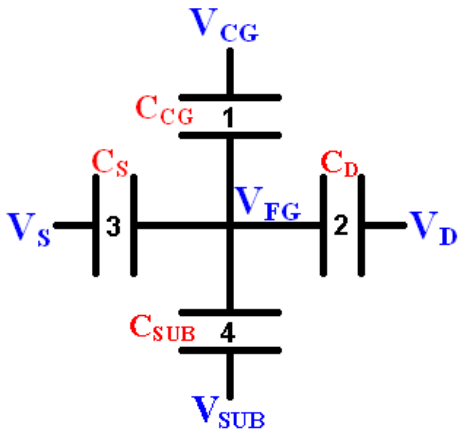


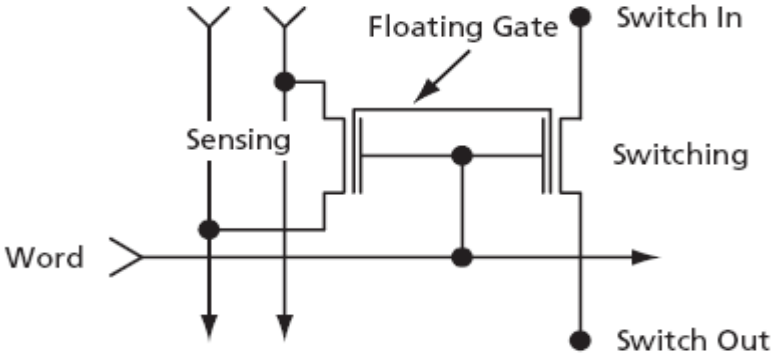
Switch Transistor Determines Whether Routing Tracks are Connected or Disconnected

Flash Cell Architecture

- In Microsemi Flash-based FPGAs, each switch transistor is accompanied by a sense transistor which shares the same floating gate and control gate
- The sense transistor is used for programming, erasing, and margining



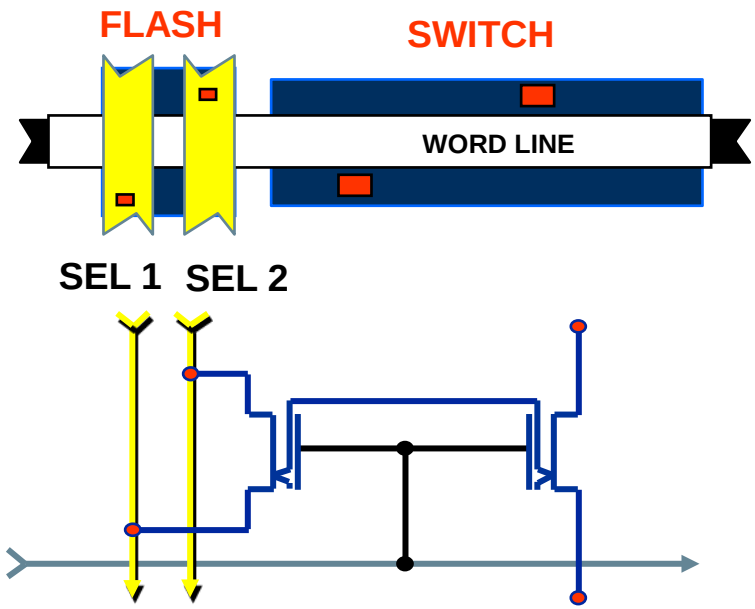


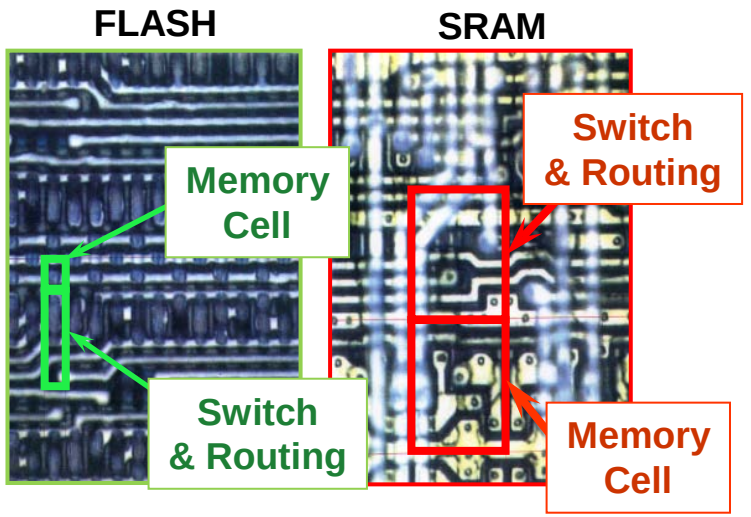


$$V = \frac{Q}{C_T} + \sum_{k=1}^{K} \frac{C_k}{C_T} V_k$$

$$C_T = C_{CG} + C_D + C_S + C_{SUB}$$

Advantages of Flash FPGA Switch



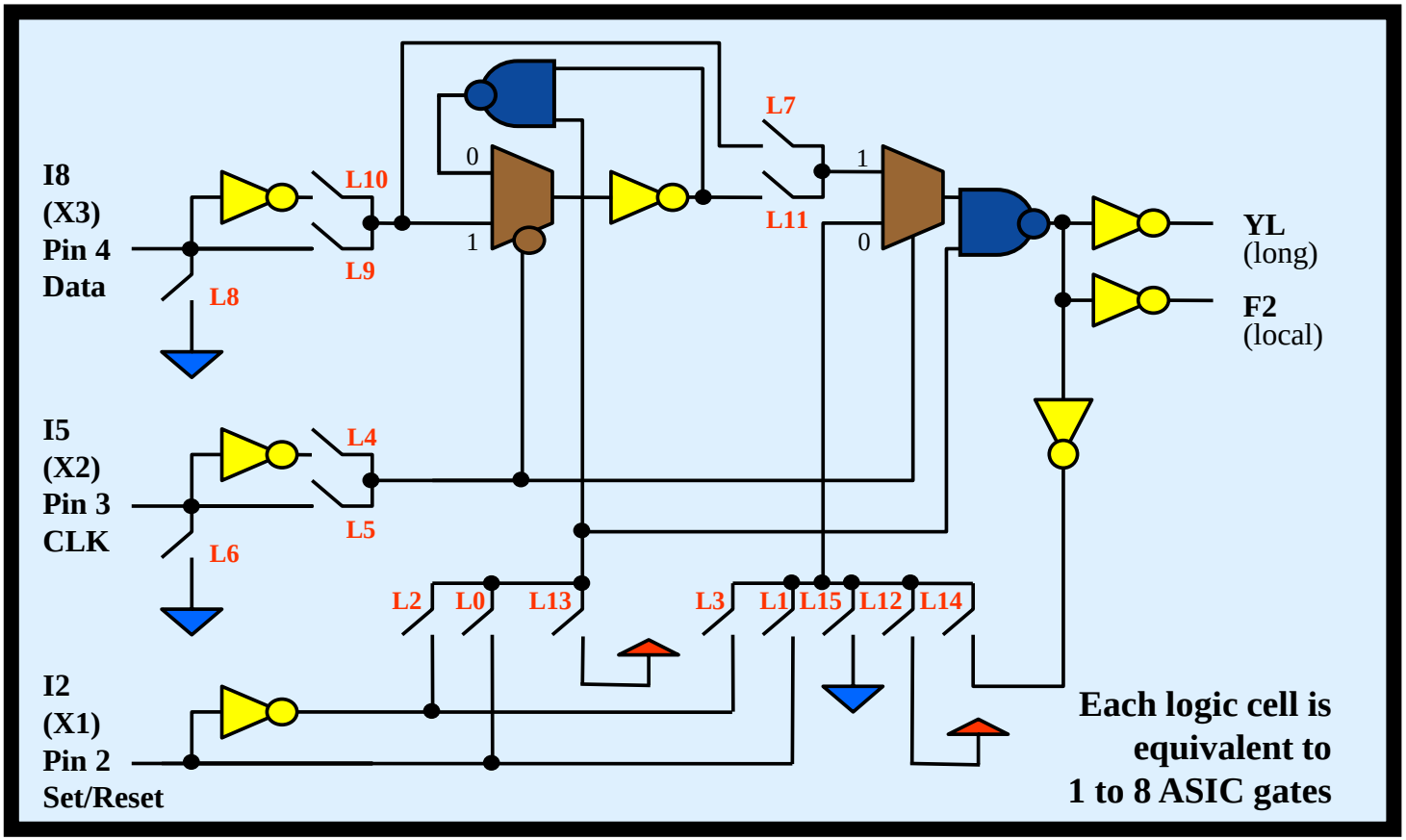


Flash Has 7 : 1 Size Advantage

- Flash FPGAs are better suited to Fuze applications than SRAM FPGAs
  - Significantly more compact – smaller package size
  - Lower power consumption
  - Non volatile – requires no external design storage device
  - Non volatile – live at power-up
  - Immune to radiation-induced upsets

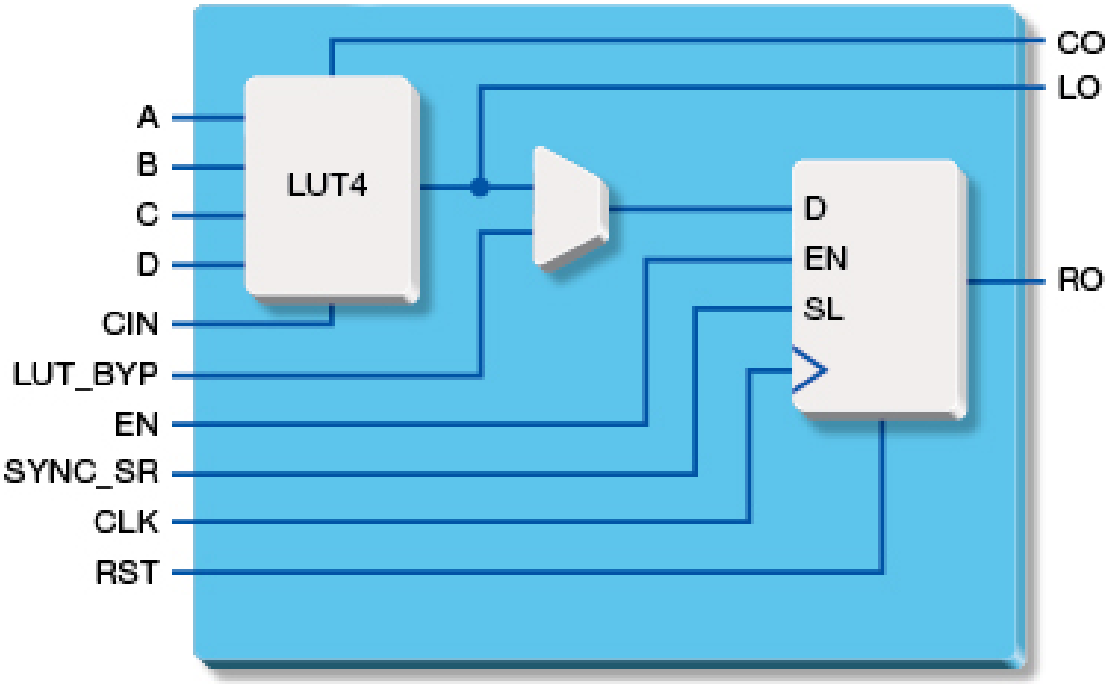
ProASIC3 Basic Logic Cell (130nm)

- ProASIC3 Logic Cell implements any 3-input combinatorial logic function or a D-type Flip Flop with enable



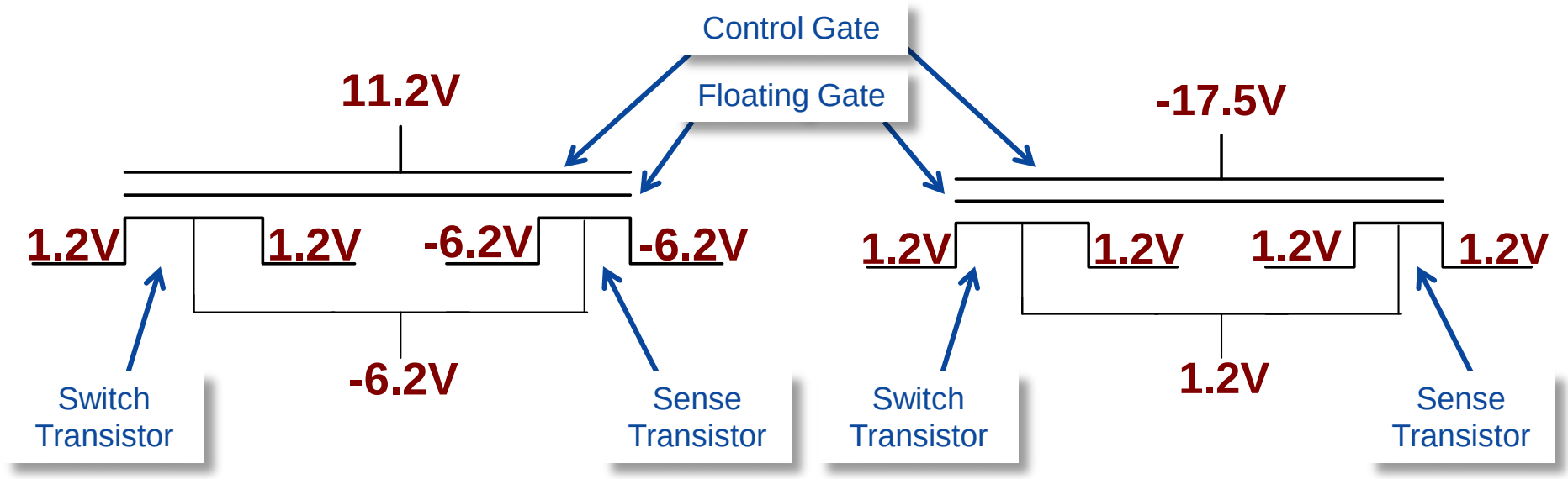
Igloo2 / SmartFusion2 Logic Cell (65nm)

- A fully permutable 4-input LUT
- A dedicated carry chain based on the carry look-ahead technique
- A separate flip-flop which can be used independently from the LUT



Physics of Program and Erase

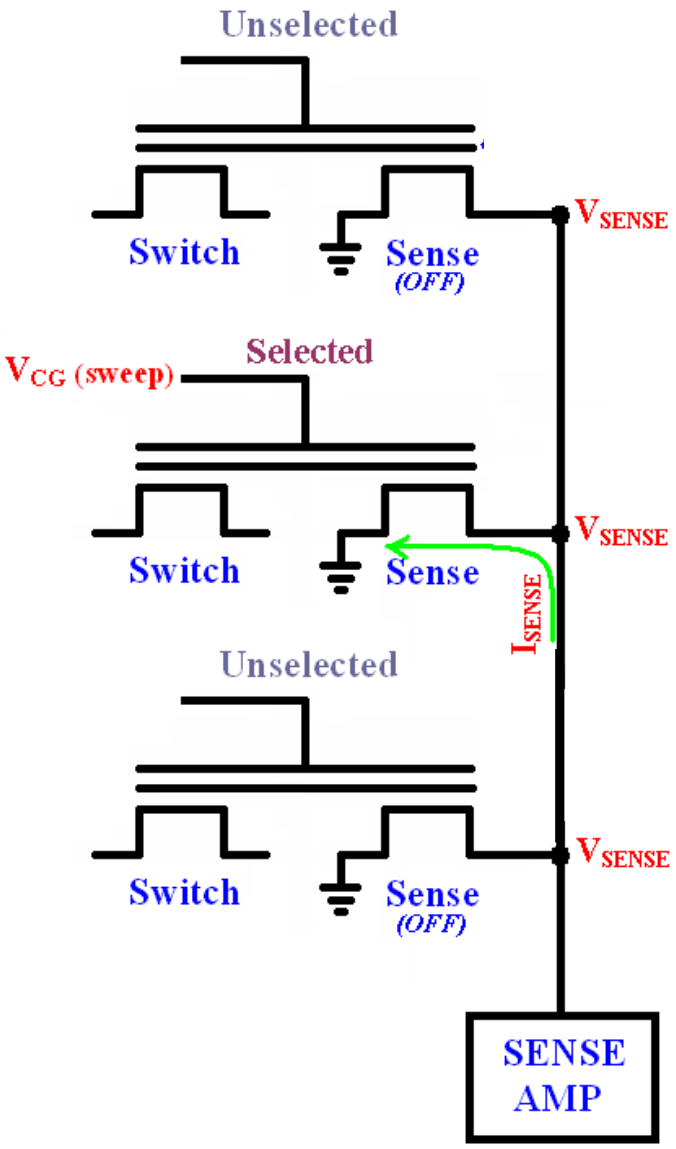
- Programming
  - Electrons injected into the floating gate
  - Floating gate becomes negatively charged
  - Switch is held in “Off” state
- Erasing
  - Electrons pushed out of the floating gate
  - Floating gate becomes positively charged
  - Switch is held in “On” state



What is Margining?

- What is margining?
  - Margining is the operation for determining the amount of charge in the flash cell
- Why do we need it?
  - In order to do any flash reliability studies, the ability to accurately track the amount of charge in a floating gate is essential
- One of the unique features of Microsemi Flash FPGAs is the ability to margin all flash cells in the FPGA fabric even after the part has been packaged

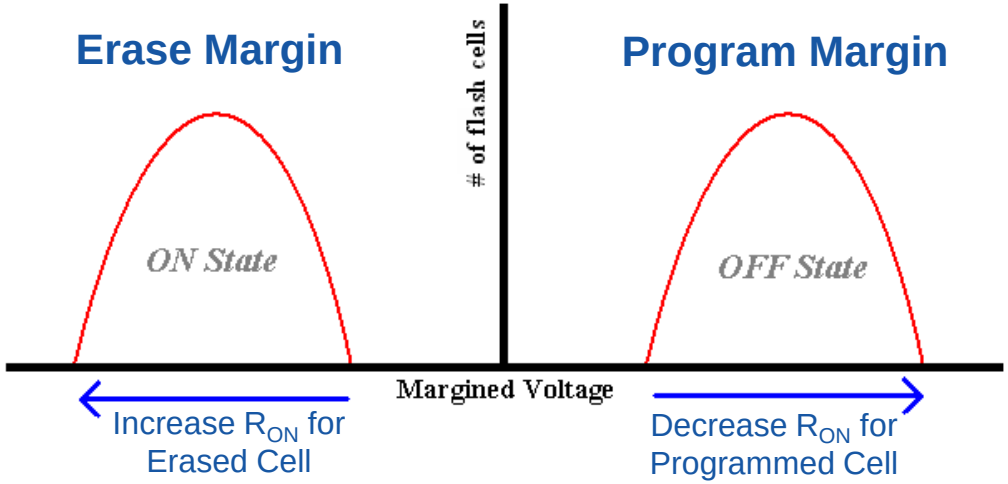
How Margining Works



- All cells are unselected to measure the leakage of the sense devices prior to margining
- V_{CG} is swept until a specific amount of current (I_{SENSE}) passes through the sense device based on the voltage (V_{SENSE}) on the column line
  - V_{SENSE} & I_{SENSE} is a reference value for defining the margined voltage of a cell

Margining Results

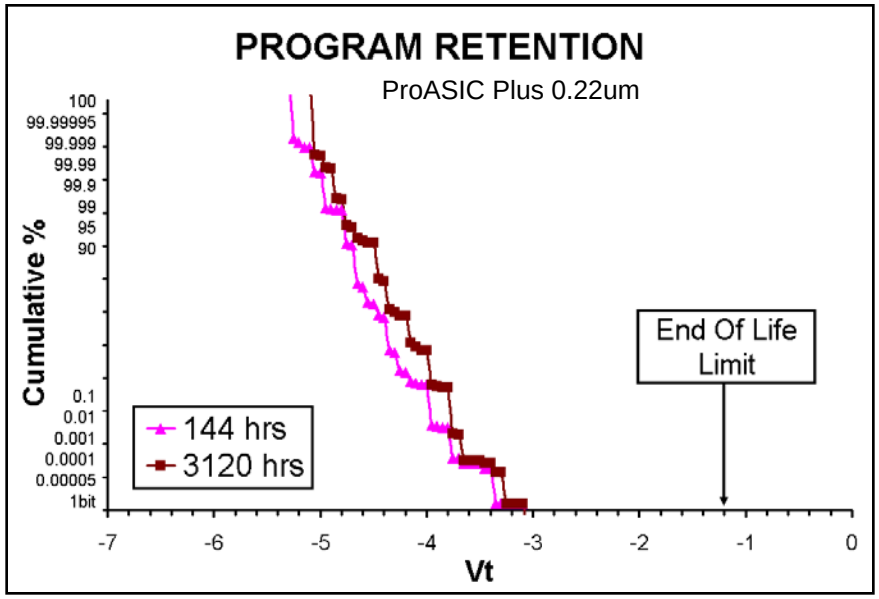
- Typical margin distribution curve

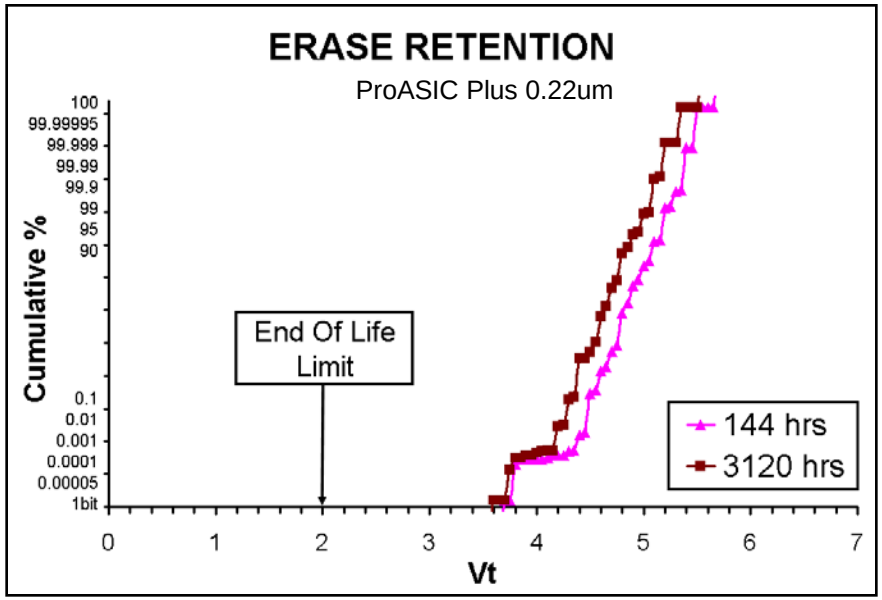


- Erased cells are in negative region
  - **$V_{FG\ (uncoupled)}$ = 1V (sense device ON)**
  - **Goal: Turn sense device OFF (increase R_{ON}) until I_{SENSE} is reached**
  - **Negative margined voltage**
- Programmed cells are in positive region
  - **$V_{FG\ (uncoupled)}$ = -1.5V (sense device OFF)**
  - **Goal: Turn sense device ON (decrease R_{ON}) until I_{SENSE} is reached**
  - **Positive margined voltage**

Reliability Studies – HTR (High Temp Retention)

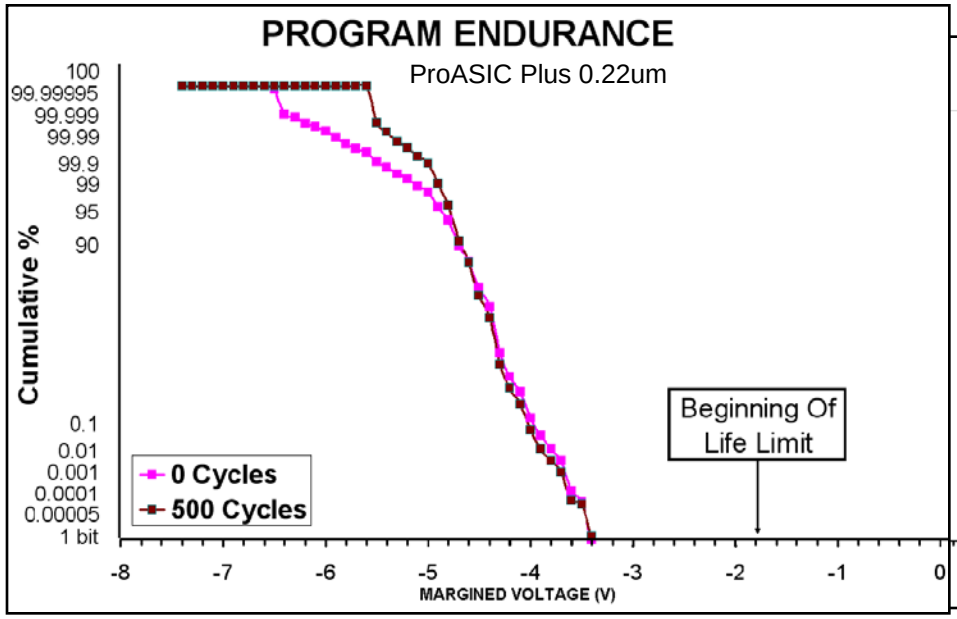
- Charges in a floating gate can leak away
  - This natural phenomenon can cause a programmed cell to become un-programmed (or an erased cell to become un-erased) in the most extreme case
  - The ability of a flash switch to maintain its charge (retention) will affect the performance/functionality of a device
- Microsemi performed HTR with a 225°C unbiased bake for 3,000 hrs (cumulative)
  - Equivalent to 23 years operation life @ 110°C junction using E_a = 0.6eV

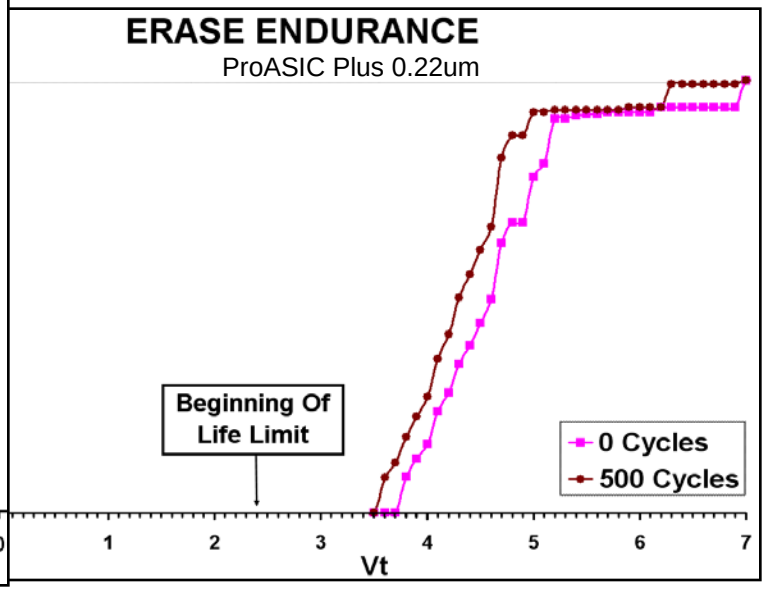




Reliability Studies – Endurance

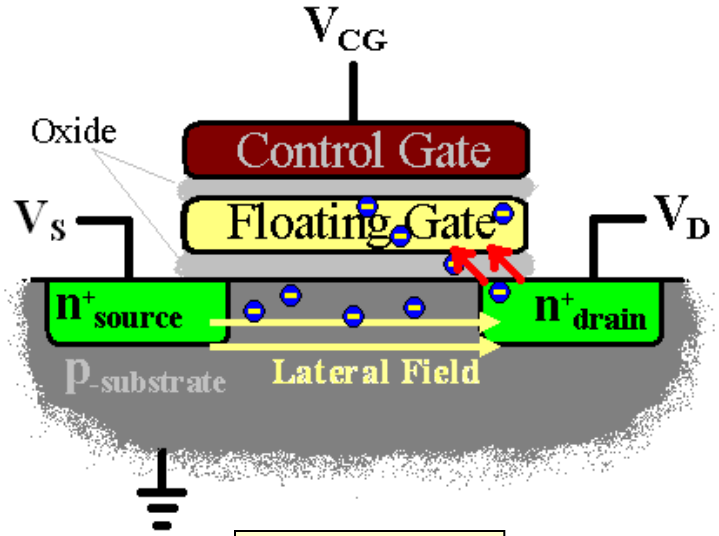
- Endurance
  - Multiple program/erase cycles can cause degradation to the NVM cell
    - Charges get trapped by the oxide as they tunnel through during program/erase, this reduces the amount of charges that can be stored in the floating gate
- Microsemi performed endurance at 25°C for 500 program/erase cycles with 100% pattern

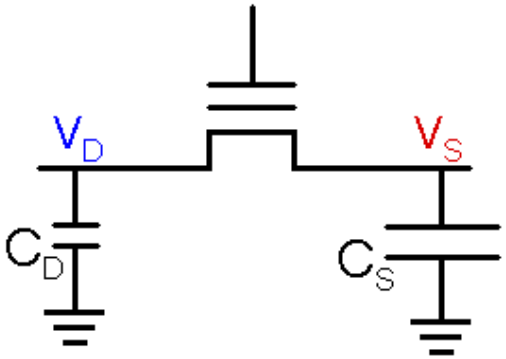


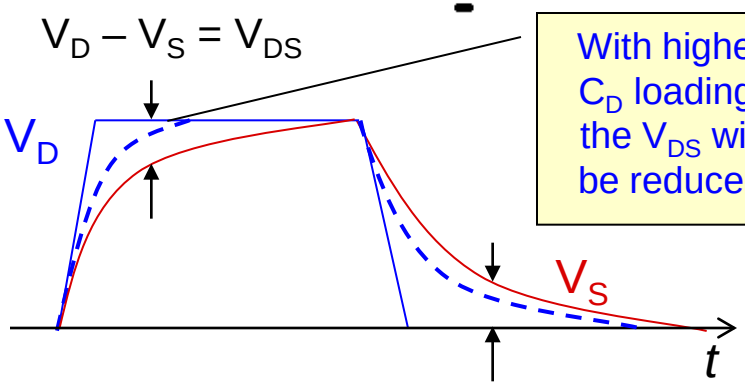


Reliability Studies – HCI (Hot Carrier Injection)

- HCI occurs when electrons get enough energy from the lateral and vertical field
  - Lateral field is dependent on V_{DS}
  - Vertical field is dependent on V_{GS}
- HCI is a mechanism used for writing flash cells
  - Unintended HCI will cause functional issue







With higher C_D loading, the V_{DS} will be reduced

--- V_D with a balance loading

- Simulations for all situations are performed to determine the V_{DS}
  - **The data collected is used to set rules for the Place & Route algorithm**
  - **Electrons must attain 3.2eV to get into the conduction band hence this is less of a concern for 130nm and 65nm Flash FPGAs relative to older generations**

ProASIC Plus (0.22um) Flash FPGA MIL-STD-883B Qualification Summary

Stress Test	Test Condition	No. of Qual Lots	# Failures / Sample Size	Test Duration Pull Point	Results
Group A	T_A = -55˚C to 125˚C, V_{DD} =2.3V to 2.7V, V_{DDP} = 3V to 3.6V, V_{PP} =V_{DD}, V_{PN} = GND (Mil-Std-883, TM 5005)	1	0/129 (+3 spares)	NA	*PASSED*
Group C	T_A = 150˚C, T_J = 160˚C V_{DD} =2.7V, V_{DDP} = 3.6V, V_{PP} =16.2V, V_{PN} = -13.6V (Mil-Std-883, TM 5005)	1	0/129 (+3 spares)	184hrs (no pull point in between)[1]	*PASSED*
Group D3/D4	-65˚C to 150˚C (Mil-Std-883, TM 5005)	1	0/15, 0/15	N/A	*PASSED*
ESD	Programmed (Mil-Std-883, TM3015)	1	0/3 (HBM)	N/A	*PASSED 1800V*
Capacitance	(Mil-Std-883, TM3012)	1	0/3	N/A	*PASSED*
Latchup	(JESD-78)	1	0/3	N/A	*PASSED*

Note 1: As an engineering study, additional 500 hours of HTOL at 125˚ C was performed on the Group C lot. No failure was observed.

ProASIC3 (130nm) Flash FPGA
MIL-STD-883B Qualification Summary

QUALIFICATION # M036			DATE: 03/30/2010
Qualification Description:	Military qualification of RT3PEL (600 / 3000) per MIL-STD-883B		
Qualification Vehicle:	RT3PE3000L	Package:	CG896
Wafer lot number:	QHR8G	Date Code:	0925
MESA Lot Number	62941039	Fab:	UMC
PCN Required?	N/A	PCN#	N/A
Qualification Results & Conclusion:			
• The RT3PEL qualification devices have passed all requirements specified in the Qualification Proposal. • Therefore, RT3PEL MIL-STD-883B is hereby qualified and is ready to be released for production.			

Qualification Results Summary

Stress Test	Test Condition	No. of Qual Lots	# Failures / Sample Size	Test Duration Pull Point	Failure Analysis Results/Mechanism
Group C (TM 5005, Table III)	T_A = 125˚C, Vcc / Vccpll = 1.575V, Vccl/VMV/ Vjtag= 3.6V,	1	0/79 (+2 Spares)	168 hrs (1st) 500 hrs (2nd) 1000 hrs (final)	PASSED[1]
Group D3/D4 (TM 5005, Table IV)	-65˚C to 150˚C	1	0/15	100 cycles	PASSED
ESD (TM3015)		1	3 (HBM)		PASSED[2]
Capacitance (TM3012)		1	3		PASSED
Latchup (JESD-78)	T_A = 125˚C	1	6		PASSED
Characterization (RT3PE3000L)	T_A = -55˚C to 125˚C	1	5		PASSED

Flash FPGA Reliability Summary

- Reliability test results are reported in Microsemi FPGA reliability report http://www.microsemi.com/document-portal/doc_download/131371-rt0001-microsemi-corporation-soc-products-reliability-report-revision-13

Reliability Summary

Table 1: **Reliability Summary: FIT Rate by Device Technology**

Device Technology	Number of CMOS Failures	Device Hours	T_J (°C)	EA, eV	Confidence	FIT	MTTF
1.0 µm CMOS FPGA	1	3.60E+08	55	0.7	60%	5.62	1.78E+08
1.0 µm CMOS FPGA (RH1020)	0	3.97E+07	55	0.7	60%	23.05	4.34E+07
0.8 µm CMOS FPGA (RH1280)	1	9.16E+07	55	0.7	60%	22.04	4.54E+07
0.8 µm CMOS FPGA	0	2.05E+08	55	0.7	60%	4.47	2.24E+08
0.6 µm CMOS FPGA	0	1.82E+08	55	0.7	60%	5.04	1.99E+08
0.6 µm RT54SX CMOS FPGA	0	2.29E+07	55	0.7	60%	39.88	2.51E+07
0.45 µm CSM CMOS FPGA	1	1.09E+08	55	0.7	60%	18.05	5.41E+07
0.45 µm UMC CMOS FPGA	0	3.80E+07	55	0.7	60%	24.06	4.16E+07
0.35 µm CMOS FPGA	0	6.31E+07	55	0.7	60%	14.51	6.89E+07
0.25 µm MEC CMOS FPGA	2	7.51E+07	55	0.7	60%	41.40	2.42E+07
0.25 µm Infineon Flash CMOS FPGA	0	3.62E+07	55	0.7	60%	25.30	3.95E+07
0.25 µm UMC CMOS FPGA	0	7.84E+08	55	0.7	60%	1.17	8.57E+08
0.22 µm UMC CMOS FPGA	0	5.19E+08	55	0.7	60%	1.76	5.67E+08
0.22 µm UMC Flash CMOS FPGA	0	8.49E+07	55	0.7	60%	10.77	9.28E+07
0.15 µm UMC CMOS FPGA	2	4.56E+08	55	0.7	60%	6.82	1.47E+08
0.13 µm Infineon Flash CMOS FPGA	0	4.56E+08	55	0.7	60%	2.01	4.98E+08
0.13 µm UMC Flash CMOS FPGA	1	2.78E+08	55	0.7	60%	7.28	1.37E+08
0.065 µm UMC Flash CMOS FPGA	0	3.64E+06	55	0.7	60%	3.22	3.11+08

0.22 µm ProASIC Plus

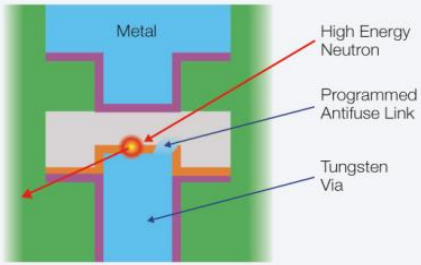
0.13 µm ProASIC3 and Derivatives

0.065 µm Igloo2 and SmartFusion2

No Configuration Failures Due To Radiation

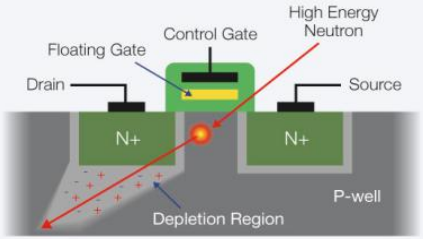
- Immunity to configuration failures due to atmospheric neutron radiation
  - Increasing problem for SRAM-based FPGAs
- Microsemi's Antifuse- and Flash-based FPGAs are immune

Antifuse FPGAs



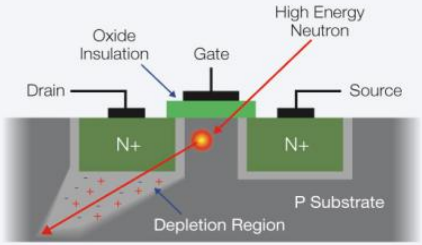
Antifuses have a permanently-programmed metallic link, which cannot be altered by energetic particles or other radiation.

Flash FPGAs



High energy particles (atmospheric neutrons, heavy ions in space) are unable to generate sufficient charge to cause the floating gate to erroneously change state.

SRAM FPGAs



Incoming neutron causes firm error in logic modules leading to

Incoming neutron causes firm error in routing matrix leading to

Weapon Effect Radiation Testing

Microsemi FPGAs for Strategic Applications

	ProASIC3 Igloo	Igloo2 SmartFusion2
Dose Rate (Upset, rad/sec)	1.4E+10	2.7E+09
Dose Rate (Survive, rad/sec)	>7.8E+10	>6.1E+10
Technology	130nm	65nm
Mil Temp Plastic	Yes	Yes
Mil Temp Hermetic	-	-
Max LE / FF	75K Tiles	146K
Max SRAM	500Kbits	4.5Mbits
Max Mathblocks	-	240

- Contact Microsemi for further information keno@microsemi.com

Industry's Lowest Power Consumption

	IGLOO nano	ProASIC3 nano	IGLOO	IGLOOE	IGLOO Plus	ProASIC3	ProASIC3E	ProASIC3L
Flash*Freeze Mode	Yes	No	Yes	Yes	Yes	No	No	Yes
Typical Quiescent Current	1.9uA	600uA	4uA	34uA	4uA	2mA	5mA	0.33mA
Static Power	2uW	0.9mW	5uW	40.8uW	5uW	3mW	7.5mW	0.4mW

- IGLOO nano offers industry's lowest power
- IGLOO family offers Flash*Freeze mode to obtain low static currents
- Flash*Freeze mode
  - Enter and exit ultra-low power mode using single pin control
  - Retains SRAM content and register data

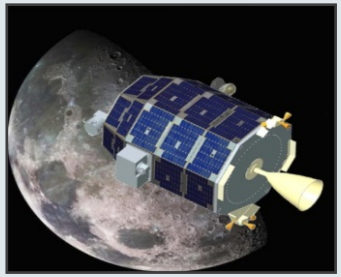
Flash FPGA Heritage

- Used in many safety-critical and mission-critical applications

Space

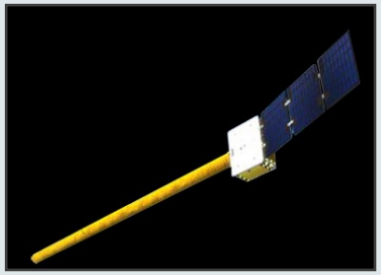
ExoMars TGO

LADEE



IRIS

Orbcomm G2



Aviation

Boeing 787

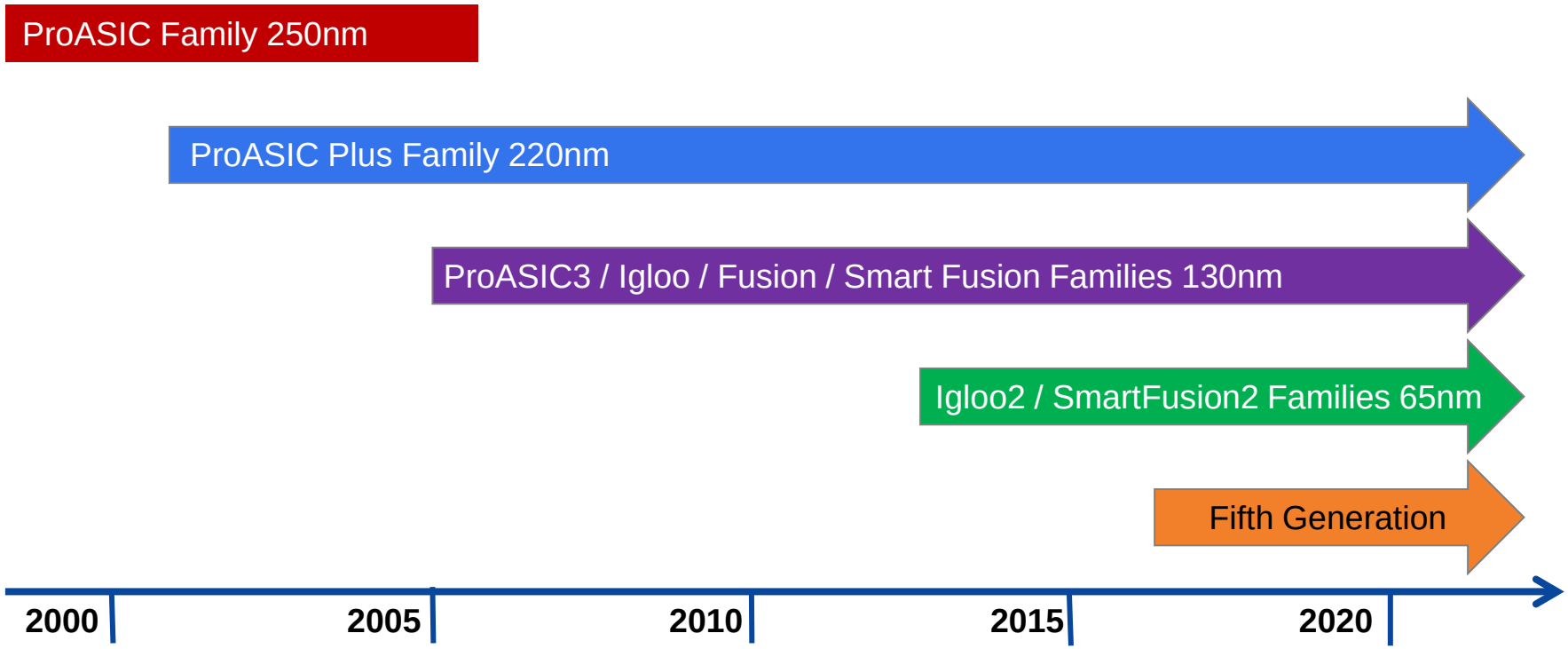
Airbus A400M

F-35 JSF

Airbus A350

Flash FPGA Outlook

- Microsemi continues to innovate new non-volatile FPGA technologies
  - Highest reliability
  - Radiation configuration upset immunity
  - Lowest power consumption



Conclusion

- CMOS FIT Rate based on HTOL data (cumulative) < 10 FIT for three most recent generations of Microsemi Flash FPGAs
  - The calculated FIT is based on 60% confidence level @ 55°C using E_a = 0.7eV
- Several device-package combinations are available with hermetically sealed ceramic packages and QML class Q or MIL-STD-883 class B screening
- Many more device-package combinations are available with plastic packaging and military temperature screening
- Reliability Studies performed to date did not reveal any potential issues with four generations of Flash FPGA
- Microsemi will continue its commitment to the Defense and Aerospace industries by delivering FPGAs with proven reliability and advanced features

Contact Information

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