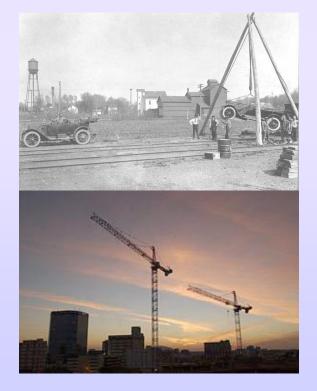




N ct everyore rects the smetcols

Which are your using? What obyour eeo?









Are you building Skyscrapers Or Dog Houses?





A Disruptive Solution to the HPC (Parallel Processing) Problem



Disruptive Solution To HPC (PARALLEL PROCESSING)



MEASURABLE GOALS:

- Provide multiple orders of magnitude improvement in application run-time speed;
- Provide an order of magnitude reduction in the time and cost to develop software;
- Allow application experts to design, build, and test software directly ;
- Allow newcomers to a project to quickly learn and understand complex software ;





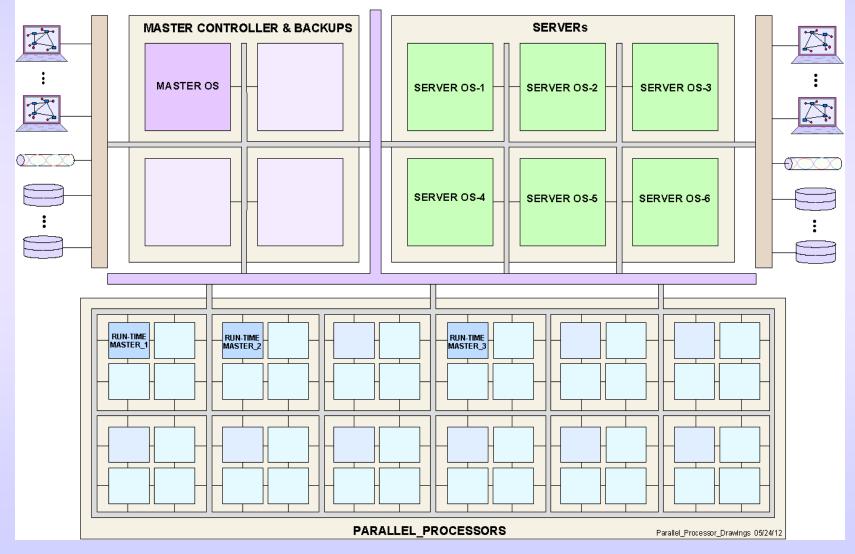
REPRESENTATIVE APPLICATIONS:

- Adaptive Control of Large Groups of Autonomous Moving Platforms
- Human Body Organ simulation
- Global Climate prediction
- Fluid Flow simulation
- Biological Particle simulation
- Chemical Molecular structure simulation
- Scanning, sorting, and correlating massive databases (Big Data)
- Weather prediction in mountainous terrain
- Power distribution simulation
- Electro-magnetic wave simulation
- Global HF power transmission
- Global Military Planning Multiple moving platform simulation





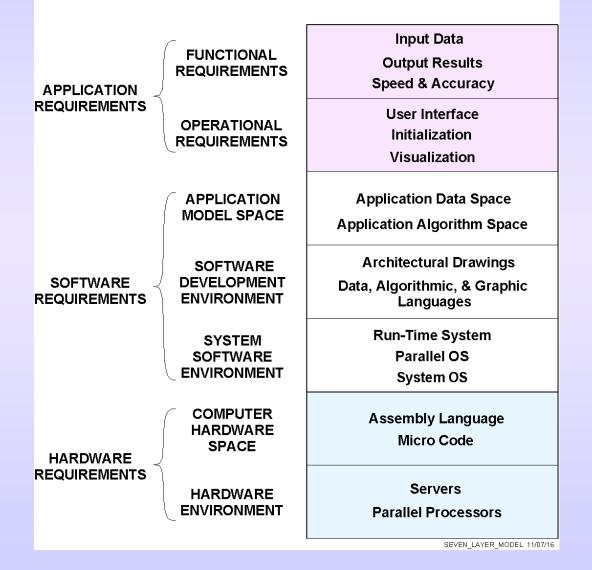
MUST DISTINGUISH BETWEEN SERVERS & PARALLEL PROCESSORS

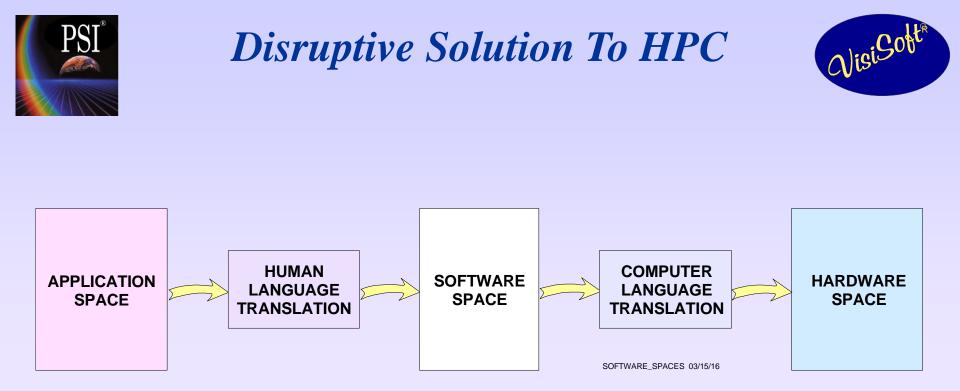






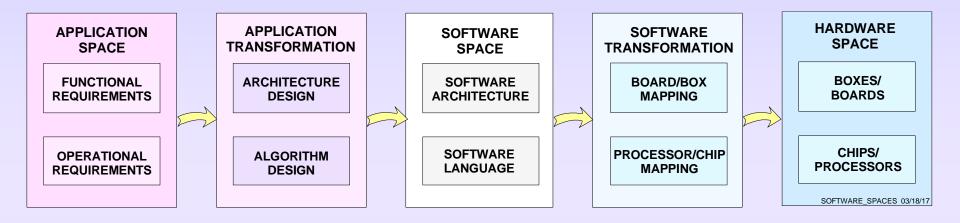
Seven Layer Model for Computer Technology





Spaces for Translation of Application Requirements into Software & Hardware





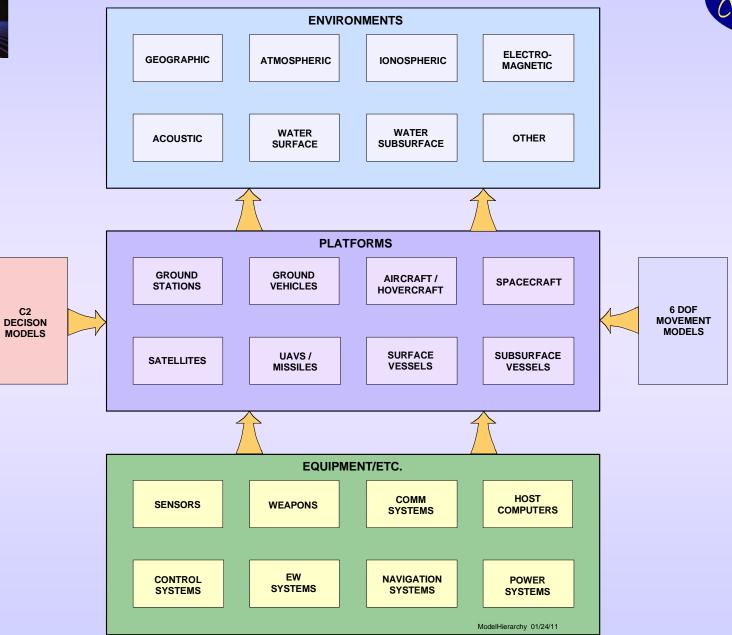
Spaces for Translation of Application Requirements into Software & Hardware

alisi Soft

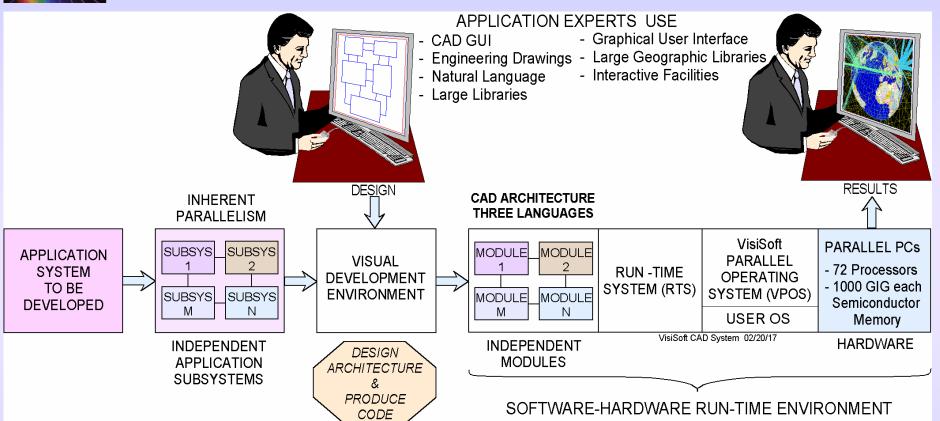


MODEL SPACE HIERARCHY









Visual Software Engineering Using A CAD System For Building Complex Software

alisiGot



RESOUR	CE: TRANSCEIVER	INSTANCES: TRANSMITTER RECEIVER
GENERAL PARAMETERS		
1	TRANSMITTER POWER	REAL INITIAL VALUE 100
1	RECEIVER THRESHOLD	REAL INITIAL VALUE 120
		_
RADIO		
1	TRANSCEIVER	STATUS TRANSMITTING
		RECEIVING
		IDLE
		OFF
1	LOCATION	
	2 X_POSITION	REAL
	2 Y_POSITION	REAL
	2 ELEVATION	REAL
	ANTENNA_HEIGHT	REAL
1	ANTENNA_GAIN	REAL
RECEIVER_CONNECTIVITY_VECTOR		
	POWER_AT_RECEIVER	REAL
	TOTAL_NOISE_POWER	REAL
1	CONNECTIVITY_MATRIX	
	2 PROPAGATION_LOSSES	
	3 TERRAIN_LOSS	REAL
	3 FOLIAGE_LOSS	REAL
	—	REAL
	2 SIGNAL_POWER	REAL
	2 SIGNAL_TO_NOISE_RATIO	
	2 LINK_DELAY	REAL
	2 LINK	STATUS GOOD
		FAIR
		POOR
TRANSCEIVER RULES		
1	TRANSCEIVER_PROCESS	RULES GOOD_RECEPTION
		CONFLICTING_RECEPTION
		CONFLICTING_BROADCAST

A Space - Data Structure (a RESOURCE)





PROCESS: RECEPTION INSTANCES: TRANSMITTER RECEIVER RESOURCES: TRANSCEIVER MESSAGE_FORMATS TRANSMITTER_OUTPUT



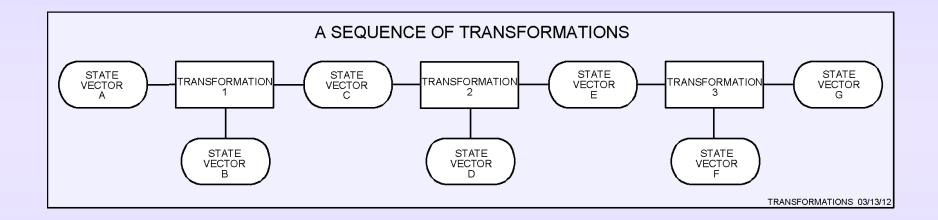
START RECEPTION IF TRANSCEIVER IS IDLE EXECUTE GOOD RECEPTION ELSE IF TRANSCEIVER IS RECEIVING EXECUTE CONFLICTING RECEPTION ELSE IF TRANSCEIVER IS TRANSMITTING EXECUTE CONFLICTING BROADCAST GOOD RECEPTION IF SIGNAL TO NOISE RATIO IS GREATER THAN RECEIVER THRESHOLD SET TRANSCEIVER TO RECEIVING ADD SIGNAL POWER TO TOTAL POWER AT RECEIVER . CALL DECODE MESSAGE . IF MESSAGE TYPE IS FORMAT A AND SYNC CODE IS VALID AND LAST_SYMBOL IS A TERMINATOR EXECUTE SEND_ACKNOWLEDGEMENT CONFLICTING RECEPTION IF POWER AT RECEIVER IS GREATER THAN SIGNAL POWER SCHEDULE ABORT RECEIVE NOW . CONFLICTING BROADCAST CANCEL END RECEIVE NOW SCHEDULE START RECEIVE IN EXPON(0.83) MILLISECONDS WITH PRIORITY 80 SEND ACKNOWLEDGEMENT MOVE ACKNOWLEDGEMENT TO TRANSMIT MESSAGE BUFFER IF DESTINATION IS BROADCAST SEARCH LINK_CONNECTIVITY_VECTOR OVER RECEIVER EXECUTING TRANSMISSION WHEN LINK IS GOOD ELSE EXECUTE TRANSMISSION . TRANSMISSION SCHEDULE LINK RECEPTION IN LINK DELAY MICROSECONDS USING TRANSMITTER, RECEIVER

A Transformation - Rule Structure (a PROCESS) ¹³





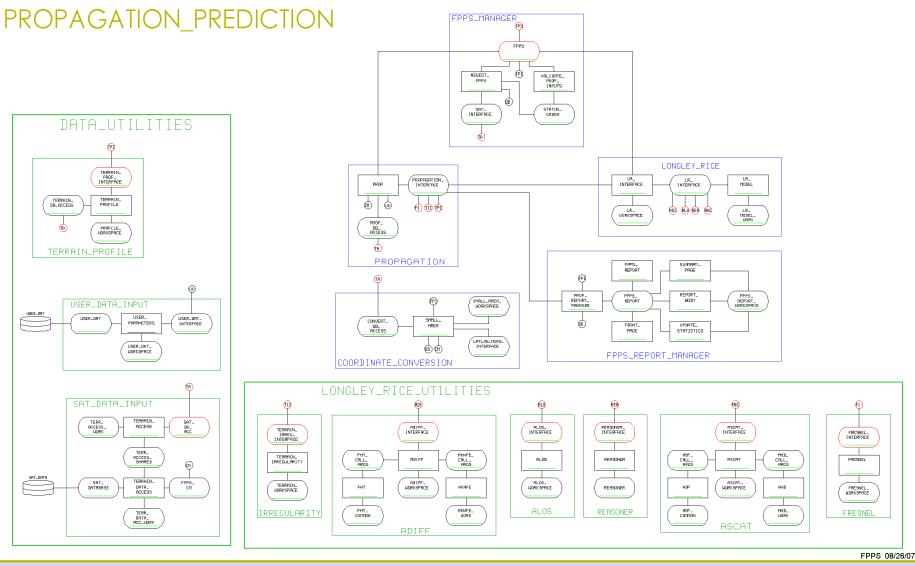
Spaces for Translation of Application Requirements into Software & Hardware



Connecting Resources & Processes to Create a Sequence of Transformations



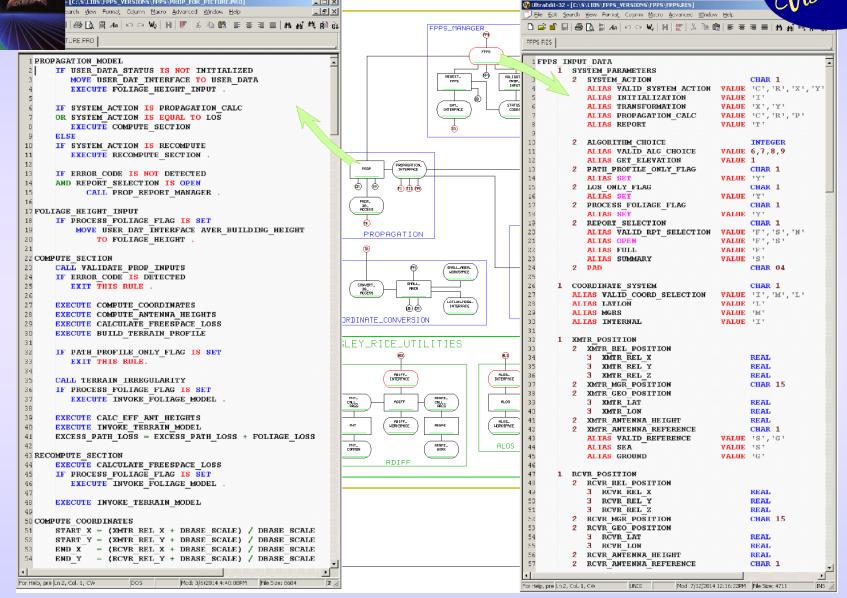




Create a Hierarchy of Software Modules

[C:\S\LIBS\FPPS_VERSIONS\FPPS\PROP_FOR_PICTURE.PRO]



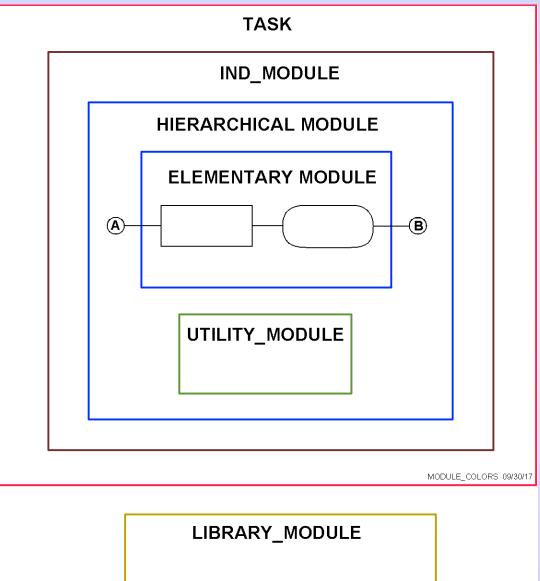


Double Click To Edit The Code

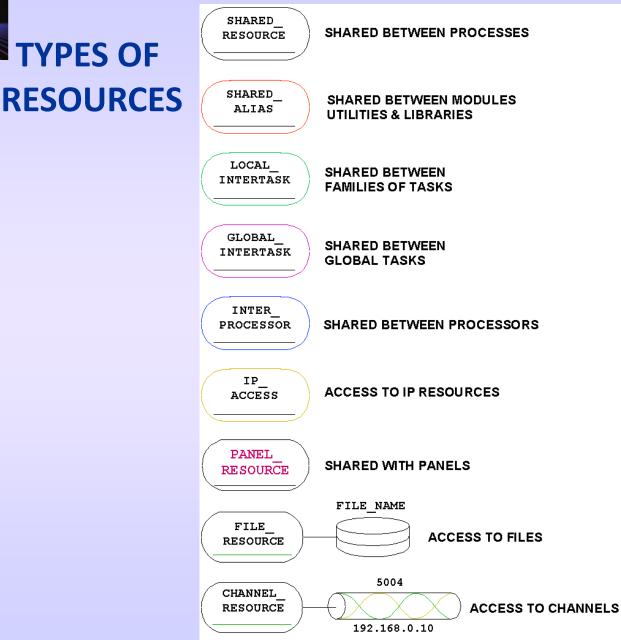


Disruptive Solution To HPC TYPES OF MODULES

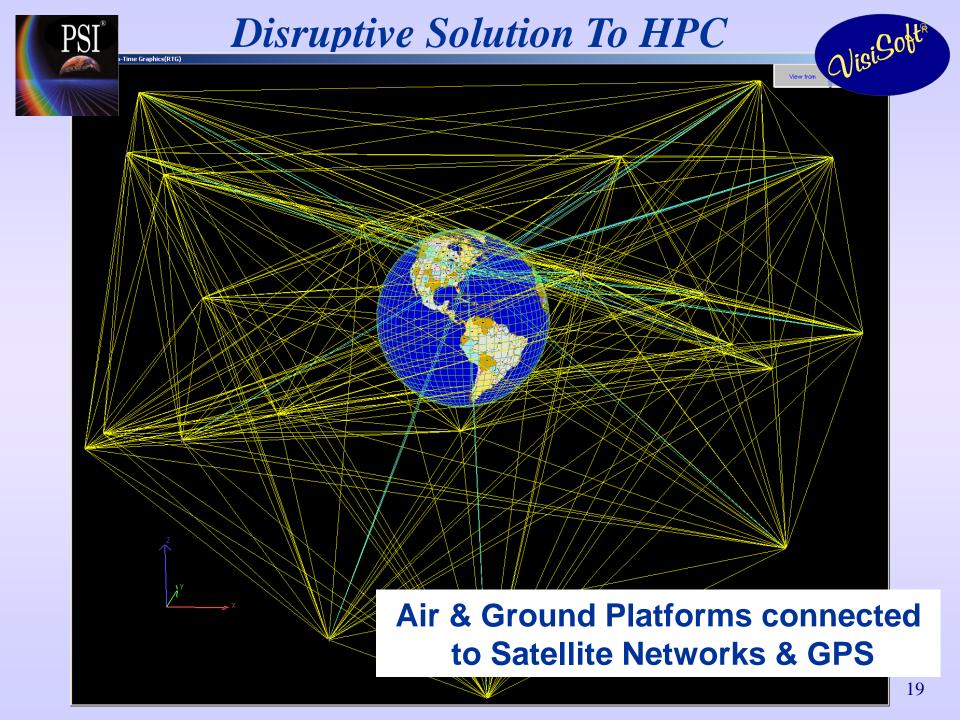




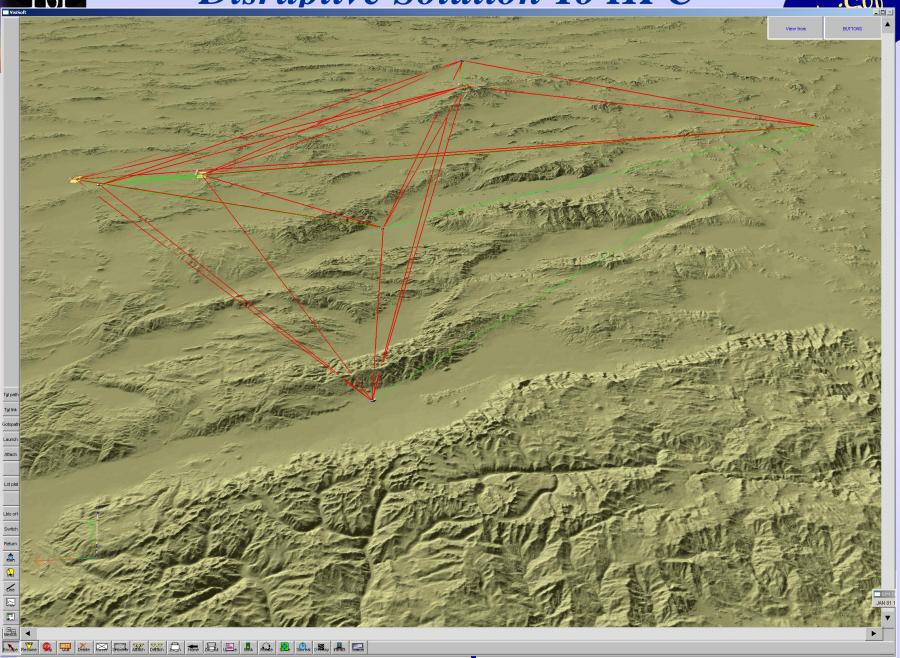
PS]

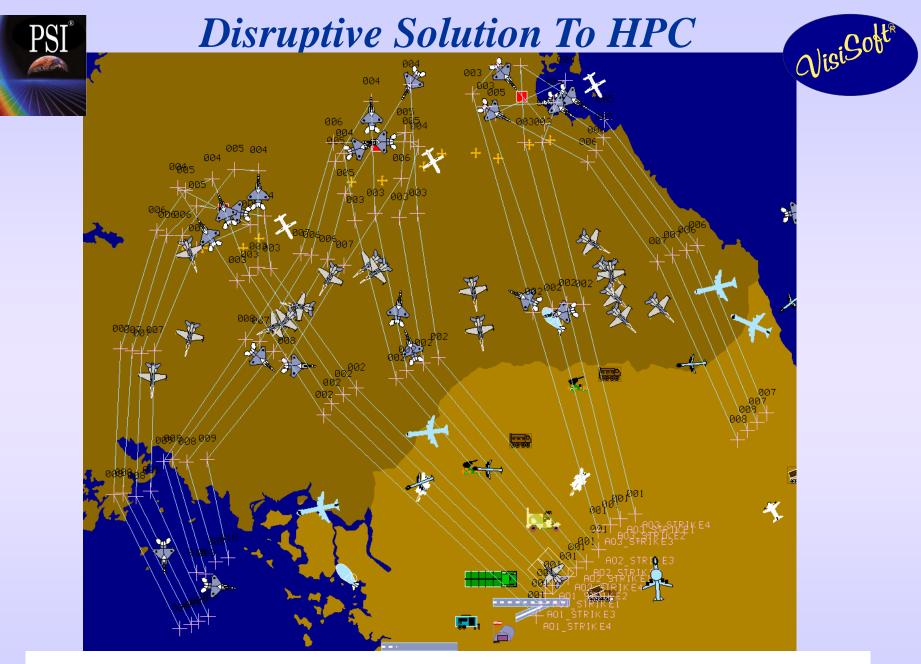






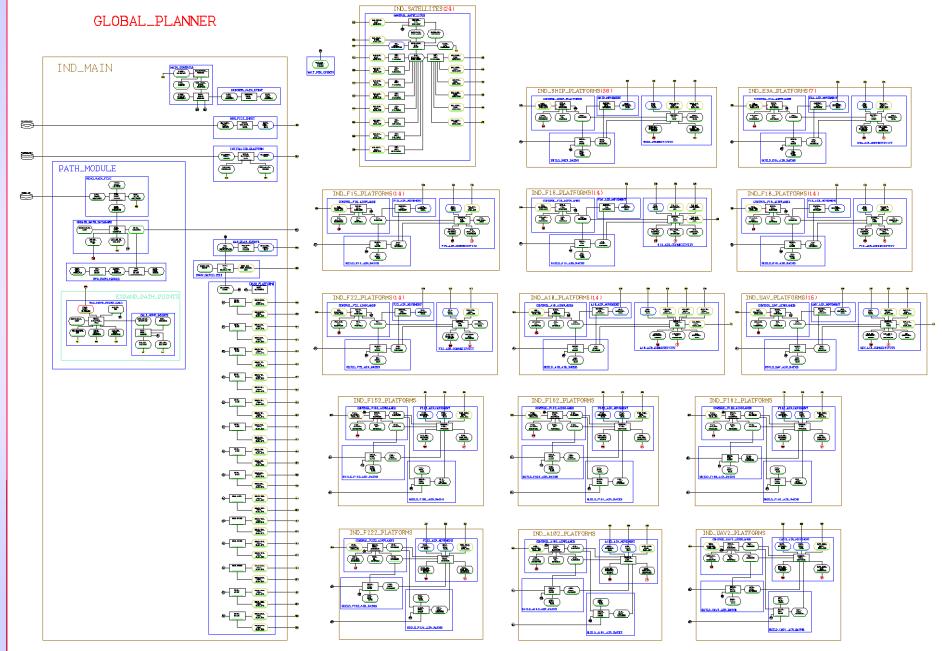






Must be able to *create* complex scenarios - fast! 21









If you use VisiSoft to build complex

Real-Time Control Systems & Simulations

on Parallel Processors

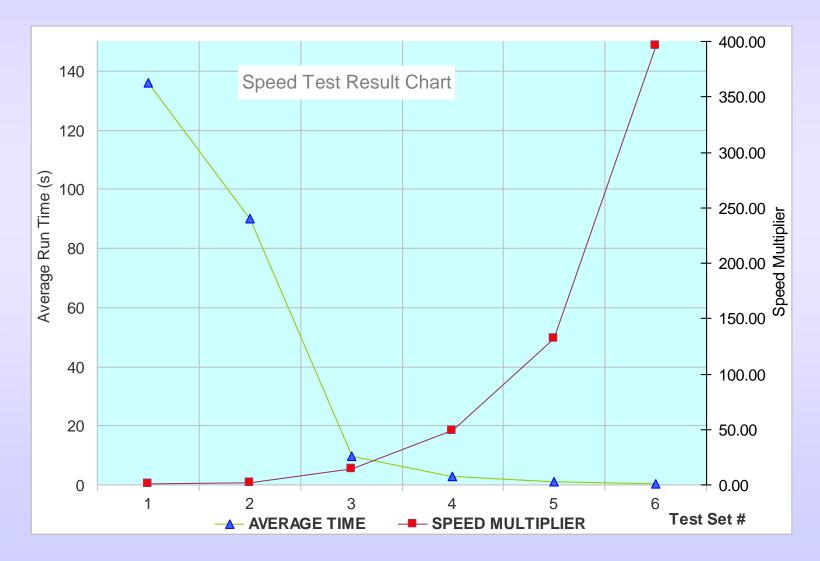
you can save many orders of magnitude

of time and money!



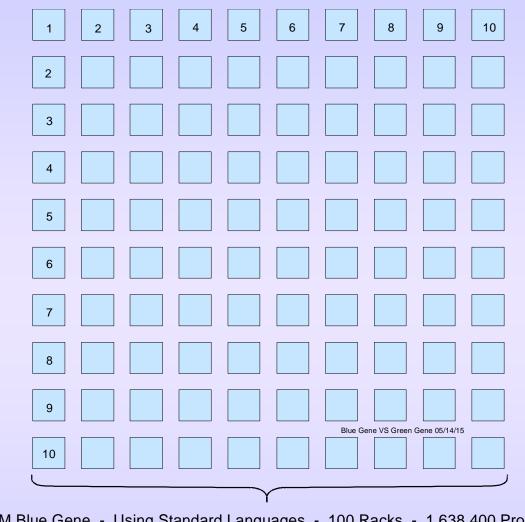


SINGLE PROCESSOR SPEED COMPARISONS - GAIN 100 X SPEED WITH VISISOFT PRINCIPLES





GO FROM 100 RACKS TO 1 RACK



The IBM Blue Gene - Using Standard Languages - 100 Racks - 1,638,400 Processors 5,000 Sq Ft. - 8,000 KW

Versus



The Green Gene Machine - Using VisiSoft - 1 Rack - 2300 Processors 16 Sq Ft. - 32 KW **WisiGoft**®





What does that do to memory boundary crossing delays?

What about 1 to 2 additional orders of magnitude?





It doesn't stop there!

We can shrink it more with our architectural drawings of software!

What about a total of 4 to 6 orders of magnitude?

Know what that does to energy utilization?





And, it doesn't stop there!

We can shrink it even more – using our hierarchical data structures to support fast heterogeneous models (time & space).

What about a total of 6 to 8 orders of magnitude* ?

Know what that does to the computer field?

*Depends on the application





It still doesn't stop there!

We can make it even faster!

Separate Parallel Processor design from Server design.

Get rid of DMA Channel Comm-Routing

And use Direct Memory Access between PC boxes.





And still - not finally,

Use VPOS - a tailored Parallel Processing OS.

And get rid of big time wasters, e.g.:

- Cache Coherency
- Thread Synchronization
- Stacks
- Etc.



Improving Speed to get Accuracy



REVIEW OF HOW THIS LEVEL OF SPEED IS ACHIEVED

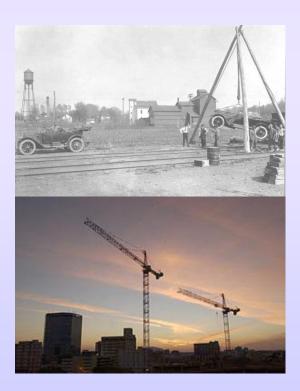
- VisiSoft SINGLE PROCESSOR SPEEDS vs C++, ..., Fortran
 - Gain 2+ Orders of magnitude (already tested)
- CAN MATCH 100 RACKS WITH 1 RACK
 - Gain 2+ Orders of magnitude (obvious distances/comm)
- VisiSoft PARALLEL PROCESSOR SPEEDS
 - Gain \approx 2 Orders of magnitude (includes PUE already tested)
- USE HETEROGENEOUS CELL SIZES
 - Gain \approx 1 Order of magnitude (already tested)
- USE HETEROGENEOUS TIME STEPS
 - Gain \approx 1 Order of magnitude (already tested)

VisiSoft - CAN BEAT REAL SPEED REQUIREMENTS BY - 6 TO 8 ORDERS OF MAGNITIDE - ON PARALLEL PROCESSORS









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E-Mail VSI@VisiSoft.com





QUESTIONS