Test Method to Evaluate High-g Component Susceptibility

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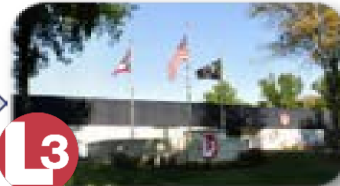
L3 Defense Electronic Systems (L3 DES)

Bulova 1923
General Time Corp 1936
KDI Precision Products 1957
Talley Industries 1970
L3 EDI 1998
L3 KDI 2001
L3 BT Fuze 2003



L3 Fuzing & Ordnance 2009

Bendix Aviation Corporation 1929
Bendix 1938
Bendix Navigation & Control Division 1966
Allied Bendix Aerospace 1983
Allied Signal 1985

L3 Space & Navigation 1999

Interstate Electronics Corporation 1956
Interstate Electronics Corporation a division of ATO 1964
Interstate Electronics Corporation a Figgie International Company 1981
Interstate Electronics Corporation – Scott Technologies 1997

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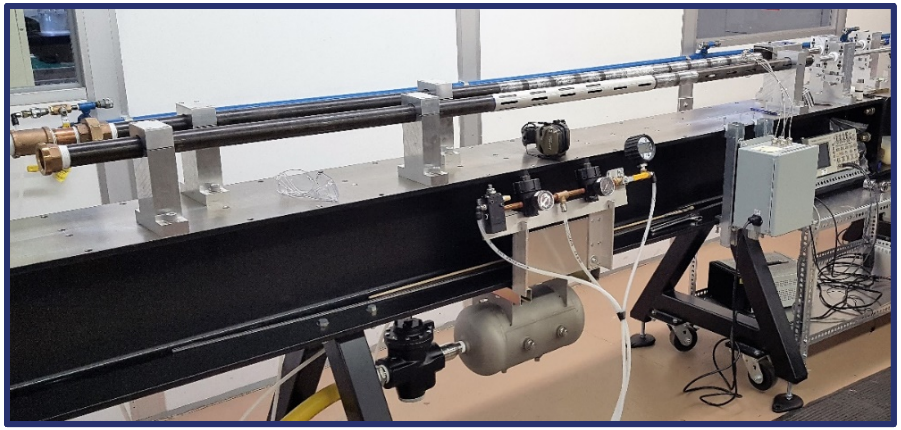
Introduction

- **Fuze level testing under severe loading conditions:**
  - **Expensive**
  - **May not identify risk early in design process**
  - **Difficult to pinpoint cause of fuze level failures**
  - **Components may function normally post-test despite intra-test failure**

The test methodology discussed here allows for a single electronic component to be tested and actively monitored during a shock event.

ESAD Electronics Characterization and Survivability

- **Single Hopkinson Bar Testing**
  - **Conduct high acceleration/high frequency testing of select electronic components**
- **Modeling of components and FEA**
  - **Correlate high fidelity FEA models of components with empirical results**



Test Set Up

- **Single Hopkinson Bar**
  - Steel Striker
  - Steel Bar
  - Threaded interface for tip
  - PCB mounted to tip with single component
  - Strain gauges
  - Laser vibrometer

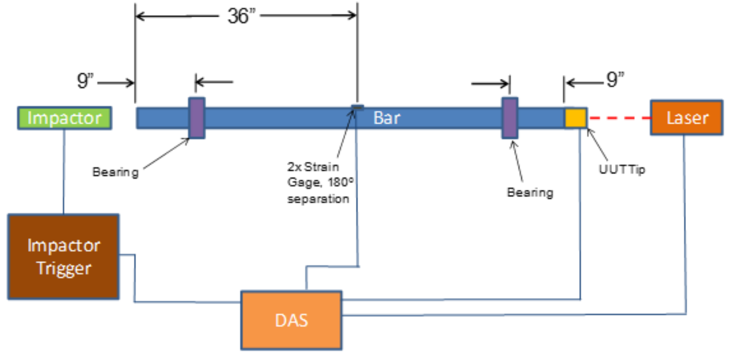


Figure 3. General Test Layout

Test Overview

- Single Hopkinson Bar testing included 3 each of 8 different components commonly used in L3 DES designs
- Tested at 3 different acceleration severity levels
  - System capable of producing pulses ranging from 1000 g's to over 250,000 g's
- Each component tested in an axial and 2 lateral configurations

Axial Lateral x Lateral y

Downselected Component List

- **Selected based on size, availability or previous history in survivable firesets**

Component Type	Description
Oscillator	Oscillator 1 - Delay block
Oscillator	Oscillator 2 - Oscillator for logic timing
Complex Logic	Complex Logic 1 - Leaded microcontroller
Complex Logic	Complex Logic 2 - Bottom terminated microcontroller
Complex Logic	Complex Logic 3 - FPGA
Discrete Logic	Schmitt Trigger
Capacitor	Capacitor 1 - Tantalum capacitor
Capacitor	Capacitor 2 - Ceramic capacitor

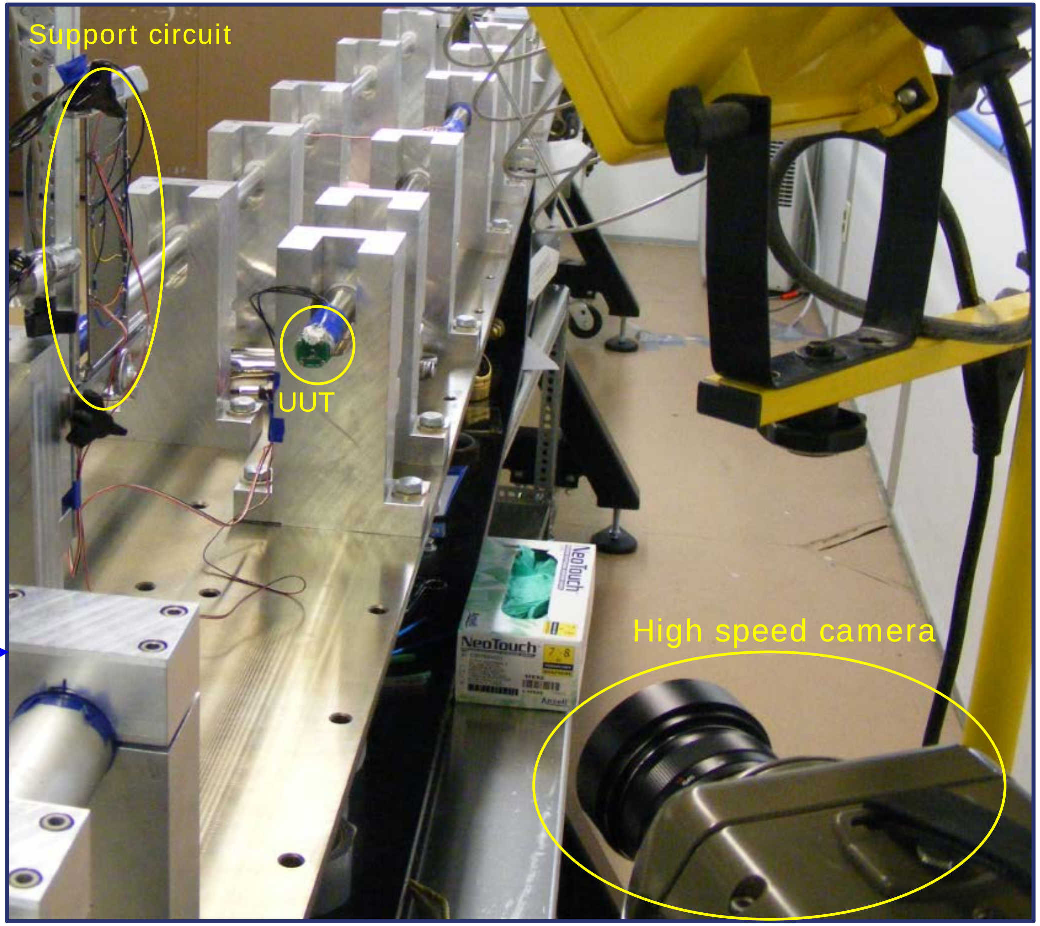
Test Methodology

- **A set of inputs was selected for each individual component in this test. The expected behavior of each component was characterized and recorded before, during, and after each test. Any change in the output was evaluated and analyzed using the appropriate failure analysis method.**
- **The output data was correlated against the strain gage derived acceleration**

Component	Input	Expected Output
Oscillator 2	5V, GND	8MHz Output
Schmitt Trigger	5V, GND 100kHz, 50% duty cycle, 0-5V	Inversion of the input
Oscillator 1	3.3V, GND 50 kHz, 75% duty cycle, 0-3.3V	Output rises 10us after input is enabled. Falls when input is falling.
Complex Logic 1	3.3V, GND	Nominal: 50kHz, 50% duty cycle Reset: 75kHz, 50% duty cycle for ~100us before resuming normal operation
Complex Logic 2	3.3V, GND	Nominal: 100kHz, 50% duty cycle Reset: 200kHz, 50% duty cycle for ~100us before resuming normal operation
Complex Logic 3	3.3V, 2.5V, GND Negative reset, 8MHz clock	Nominal: 125kHz, 50% duty cycle Reset: 500kHz, 50% duty cycle for ~100us before resuming normal operation
Tantalum Capacitor	19kHz, 20% duty cycle, 0-5V	RC charging triangular waveform from 0V to around 3.2V depending on capacitance
Ceramic Capacitor	800Hz, 20% duty cycle, 0-5V	RC charging triangular waveform from 0V to around 3.2V depending on capacitance

Test Setup

Laser vibrometer protection



Results Summary

Key	
Measured Test Severity	
Unaffected	Affected During Test
Affected Post Test	Part Failed
Test Not Conducted Due to Previous Failure	

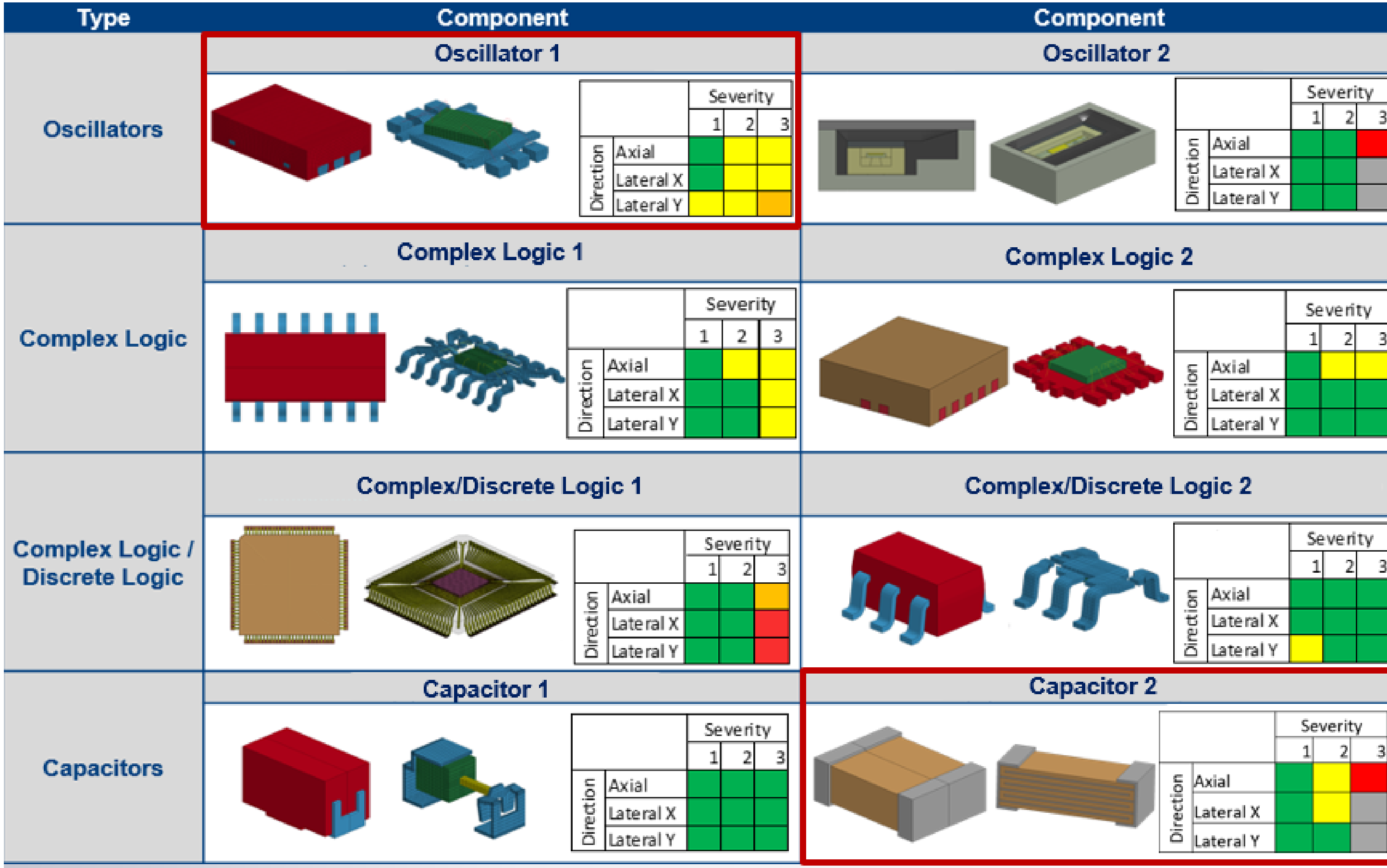
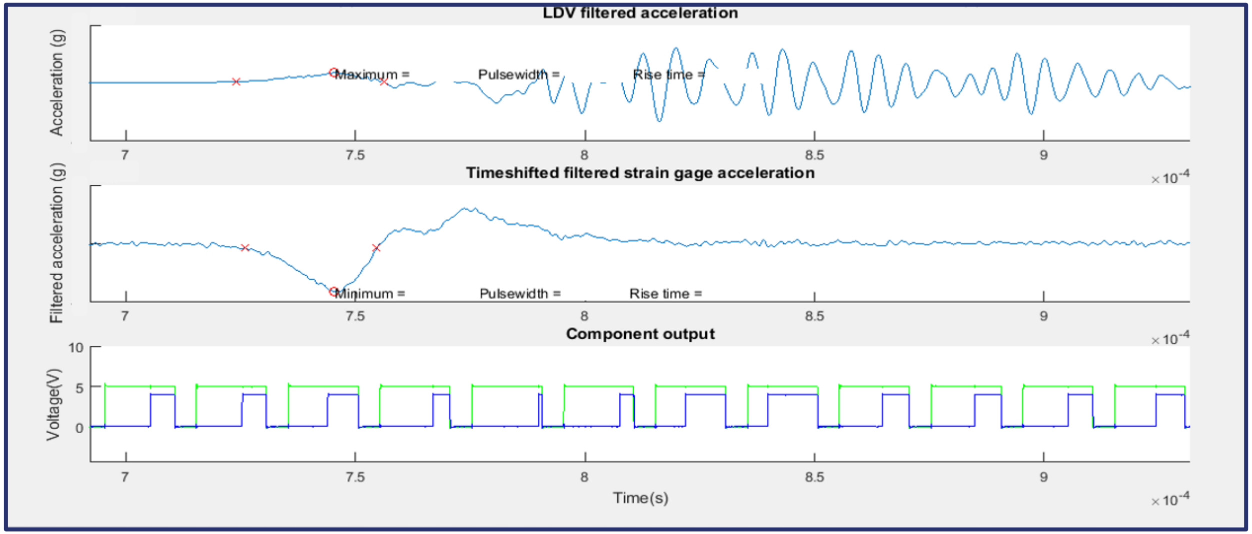


Image from ARA

Oscillator 1 – Axial Impact at Severity Level 3



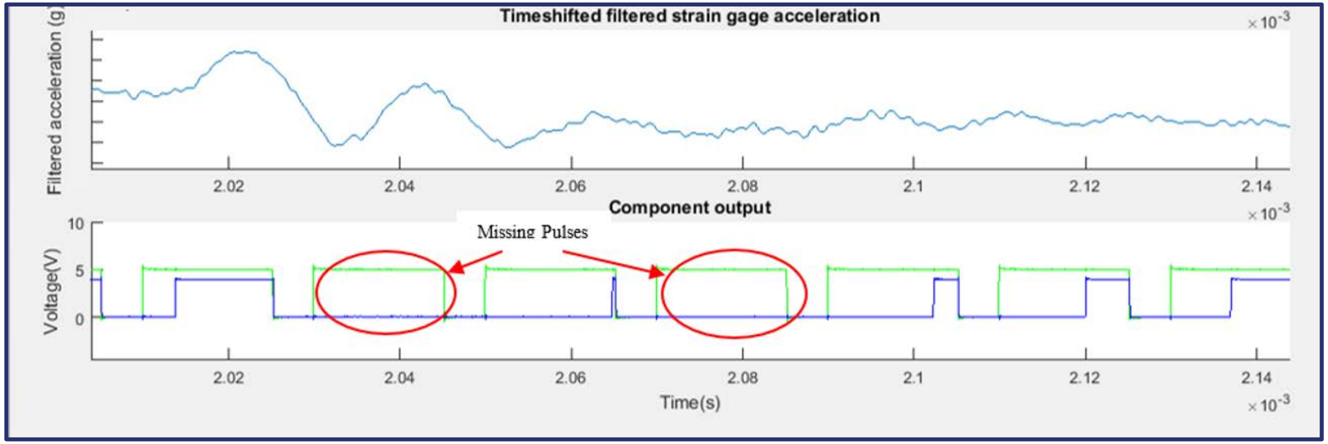
Round 3 Axial Configuration

		Severity		
		1	2	3
Direction	Axial			✖
	Lateral X			
	Lateral Y			

Green = input
Blue = output

- **Delays both greater and smaller than the expected 10us can be observed in the above figure.**
- **In the current setup for a 10us delay, a delay shift as great as ~70% can be observed in an individual pulse. It's unlikely this delay shift would scale in a 10ms set up.**
- **Further testing is required to verify this claim.**

Oscillator 1 – Lateral Y at Severity Level 3



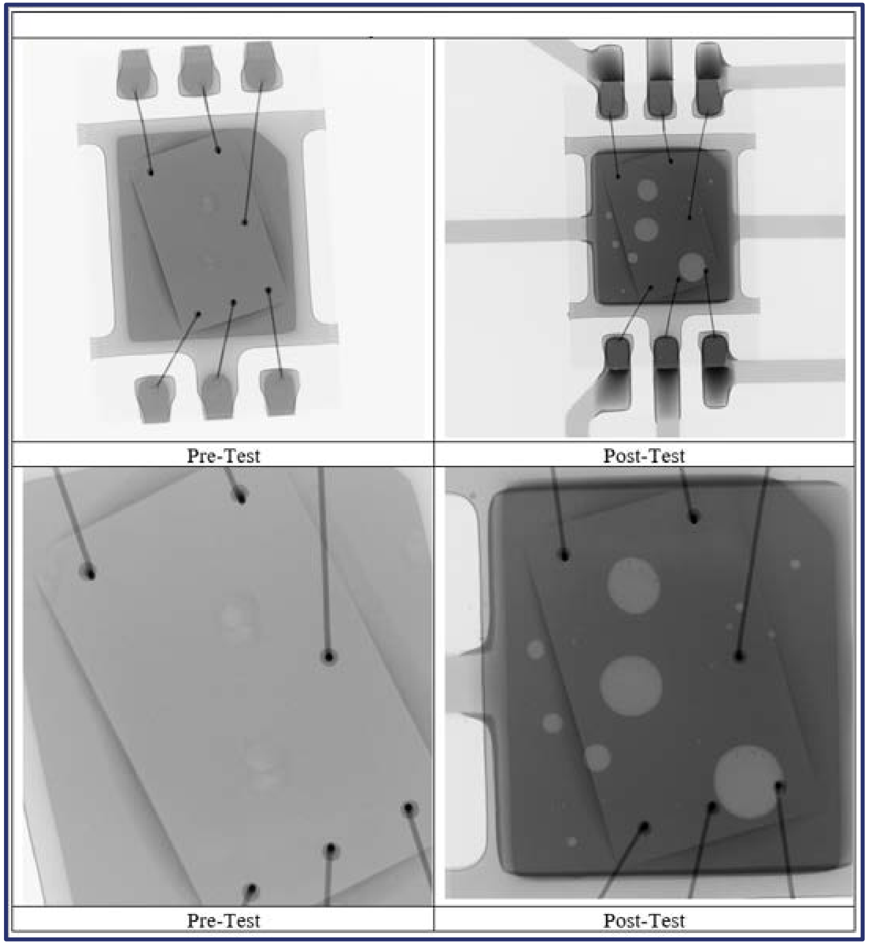
Round 3 Lateral Y Configuration

		Severity		
		1	2	3
Direction	Axial			
	Lateral X			
	Lateral Y			✖

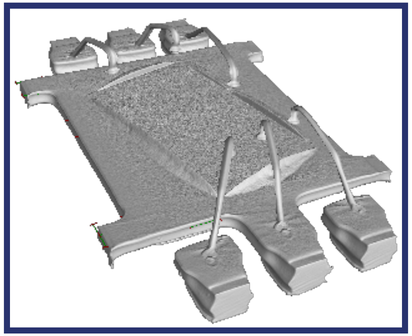
Green = input
Blue = output

- **Missing pulses indicate component malfunction**
- **Component showed a small, permanent increase in on-time pulse width after the test**

Oscillator 1 – Post Test Imaging

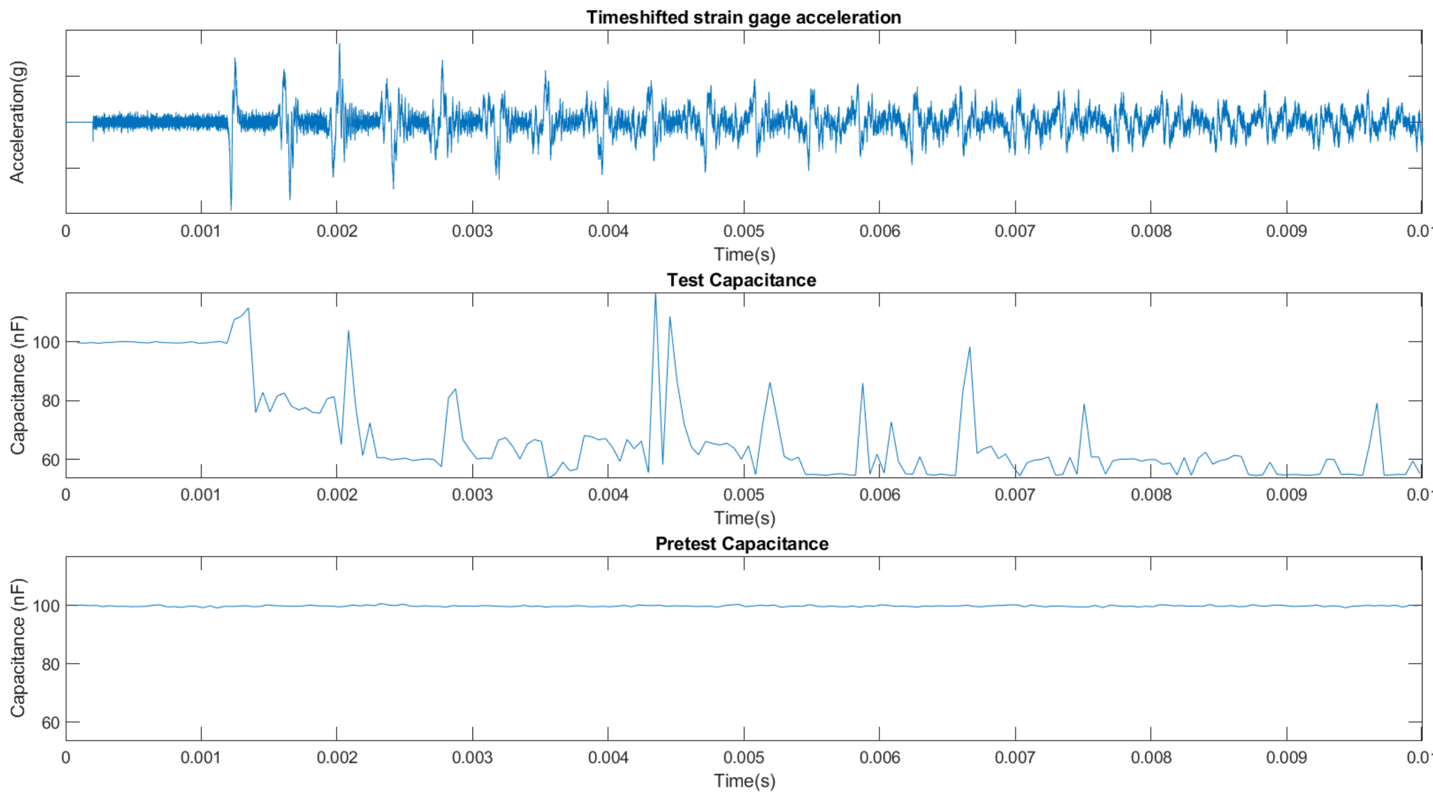


- Pre and post-test high resolution x-rays were conducted on all components
- Internal bond wires appear to be intact



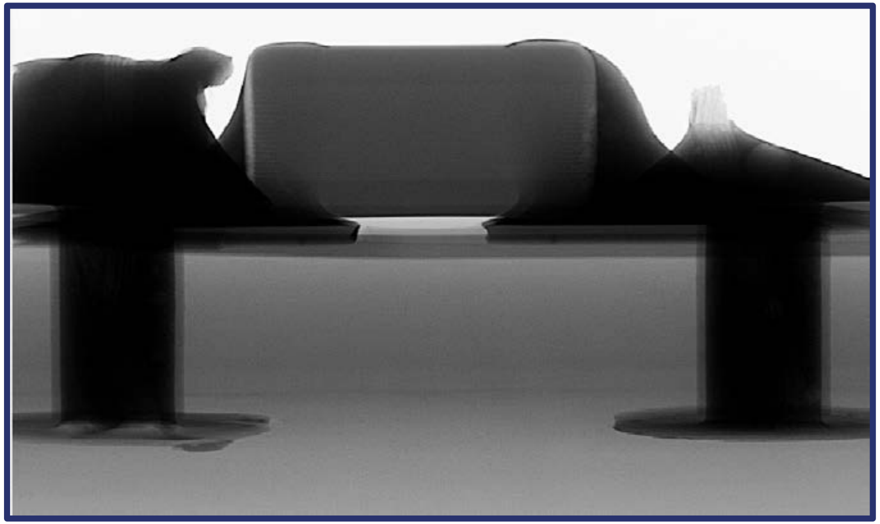
- CT Scans also conducted to better understand internal geometries

Ceramic Capacitor – Axial at Severity Level 3



Ceramic Capacitor		Severity 1	2	3
Direction	Axial			
	Lateral X			
	Lateral Y			

Ceramic Capacitor – Axial at Severity Level 3



	Computed Capacitance (nF)			
	Min	Max	Mean	Standard Deviation
Pre-Test	105.57	106.86	106.32	0.232
Test	55.70	117.63	71.34	17.56
Post-Test	61.37	62.15	61.69	0.145

- **42% decrease in capacitance was observed**
- **High resolution x-rays were not able to identify damage within capacitor layers**

Component Testing Summary

- **Developed enhanced methodology for assessing component susceptibility to high shock environments**
- **Evaluated several classes of components commonly used in ESADs**
- **Actively monitored single components during a shock event**
  - **Permits assessment of risk during High-g events that is not possible with pre and post test interrogation only**

Acknowledgements

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