



21st Annual National Defense Industrial Association
Systems and Mission Engineering Conference

Long-Term Strategy for DoD Assured Microelectronics Needs and Innovation for National Economic Competitiveness

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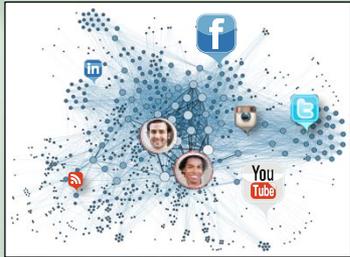
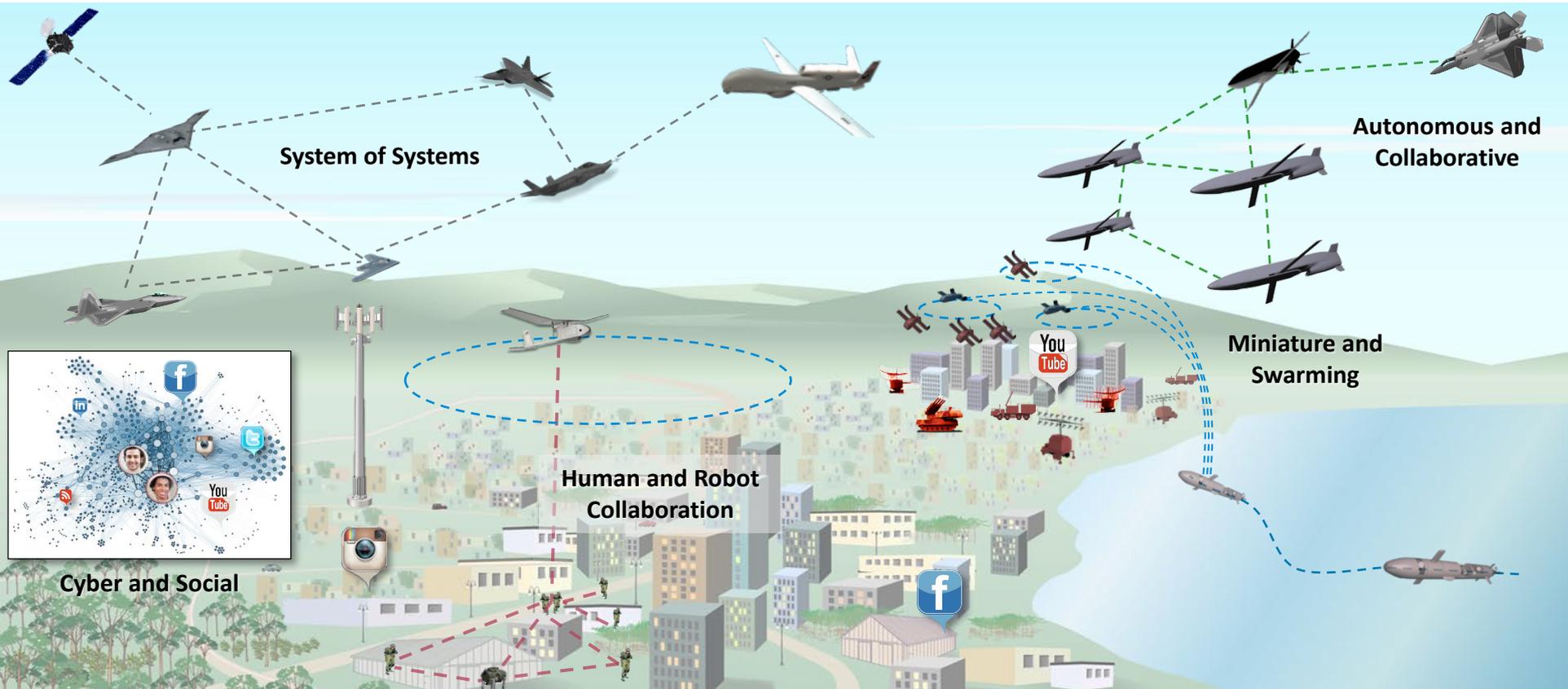
Office of the Under Secretary of Defense for
Research and Engineering

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Future Defense Systems

Advanced Microelectronics Needs



Cyber and Social

Big Data and AI Systems

Artificial Intelligence (AI) and Graph Processors

- 100B-1T node graphs
- Need 1000x performance and efficiency for real-time

Decentralized Systems

Open and Distributed Architecture & Processing

- Local processing raw data
- Rapid tech. insertion & upgrades using SotA

Human and Robot Systems

Vision, Semantic and Navigation Processing

- High performance imagers & local processing circuits
- Robust Navigation & local semantic processing

Diverse Protected Links

Frequency and Antenna Diversity Signal Proc.

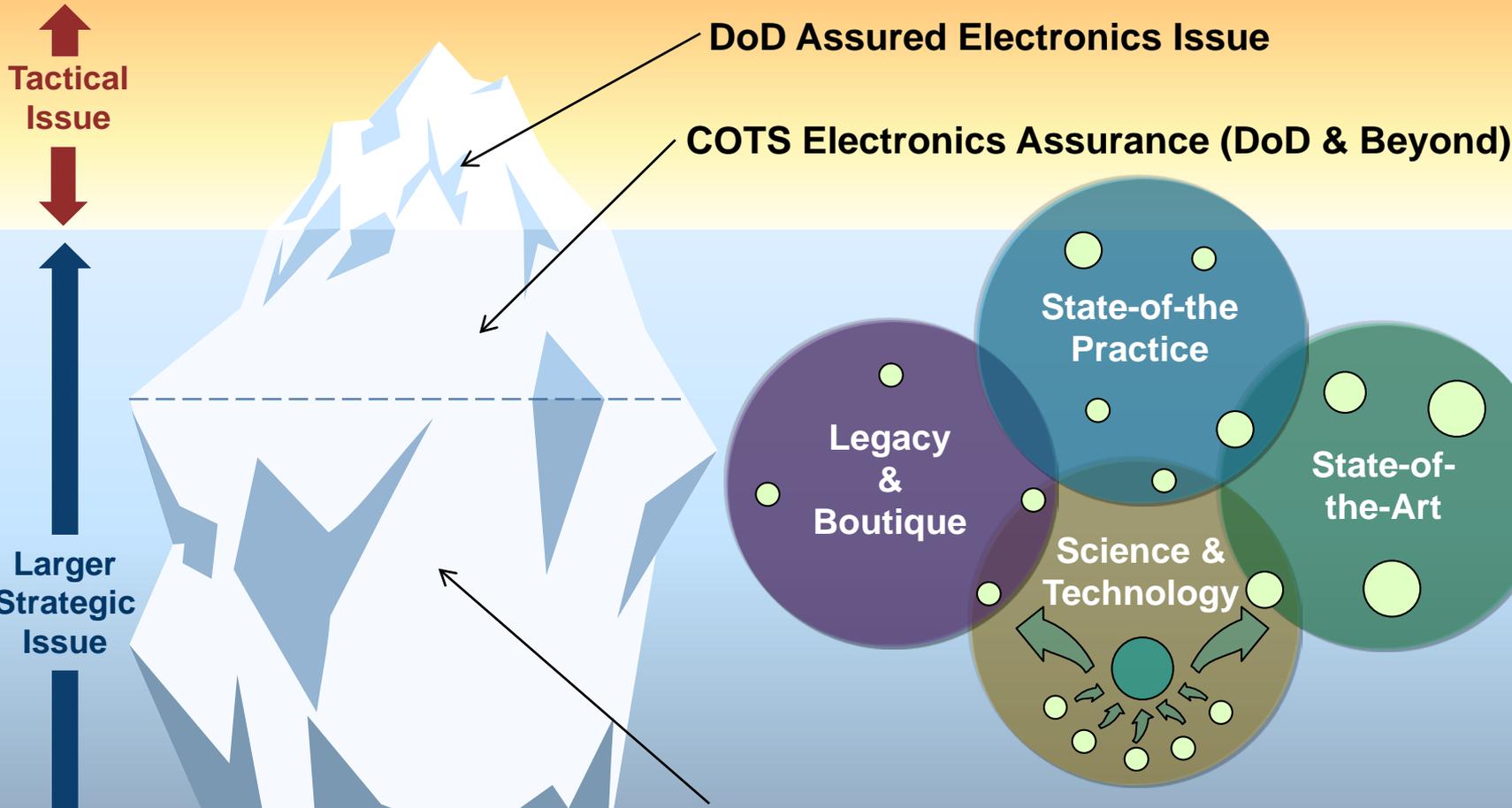
- Multi-antenna & frequencies
- Adaptive processing (Trillion Ops/sec/watt) for robust comm. & radar systems

Global Tech and Infrastructure

Leverage & Assure Access to the best Technology

- Use best global tech where it exists
- Assure domestic sources for state-of-art

Electronics as a Strategic Issue



DoD Assured Electronics Issue

COTS Electronics Assurance (DoD & Beyond)

FY03-16
Trusted
Foundry
Program

FY 17-23:
Trusted &
Assured
Micro-
electronics

FY 19-23
and beyond:
DoD Micro-
electronics
Innovation
for National
Security
(MINSEC)

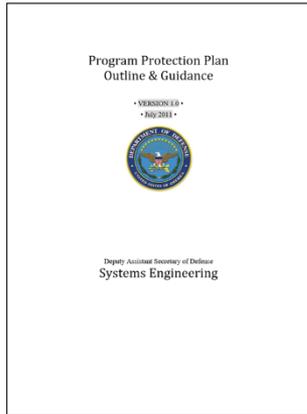
Assured access to domestic semiconductors (CMOS, analog, compound semiconductor, memory, design tools, intellectual property, manufacturing tools, processors and applications) to ensure national security & economic competitiveness

Elements of a Strategy for Ensuring Access to Assured Microelectronics

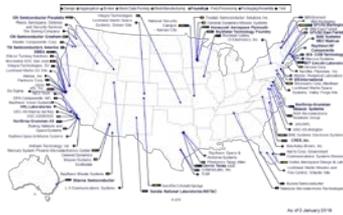


- Revised trust and assurance policy to address state-of-the-art (SOTA) technology applications, use of commercial parts in DoD systems, and full life cycle vulnerability protection, beginning with secure design and protection of intellectual property (IP)
- Healthy microelectronics verification and validation (V&V) capability
- Access to DoD/Government-unique needs, radiation-hardened by process and radiation-hardened by design technologies, in support of space and nuclear modernization, including Diminishing Manufacturing Sources and Material Shortages (DMSMS) foundry-of-last-resort capability
- Adequate workforce expertise and engagement with academia, Defense Industrial Base (DIB), and DoD user communities in prototyping, and development activities to build a domestic knowledge base for design and manufacturing of advanced microelectronics
- Research and Development (R&D) investment to lead development of the next generation microelectronics and protect domestic leadership
- Modernization to deliver modern application-specific integrated circuits (ASICs) and systems-on-chips (SOCs), reduced reliance on legacy parts and replace obsolete systems, and enactment of acquisition policies that promote rapid modernization, standards and best practices to facilitate V&V, supply chain risk assessment, and counterfeit detection
- Availability, Access and Assurance at multiple domestic SOTA Foundries and business models to sustain growth and commercial competitiveness

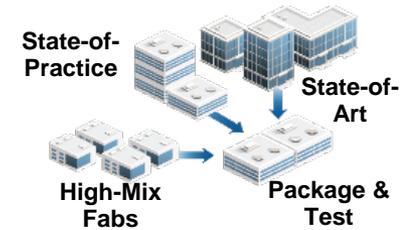
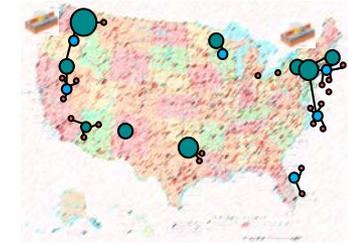
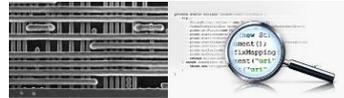
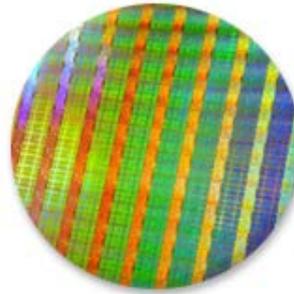
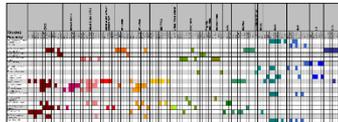
DoD Strategy and Actions



Trusted Supplier Accreditation



TAPO



Policy

- Program Protection Plan (PPP), DoDI 5200.44, ITAR, DPA Title III updates
- Strategy/Directive for Assured Microelectronics
- National Security Strategy priority



DMEA

- Maintain and expand the number of trusted suppliers
- Provide access to state-of-the-art trusted flow (TAPO)
- Support sensitive needs and operations

Trusted & Assured Microelectronics

- Assured Access to state-of-the-art foundries through modern trust and assurance methods and demonstration
- Industrial standards for assurance
- Joint Federated Assurance Center Enhancement

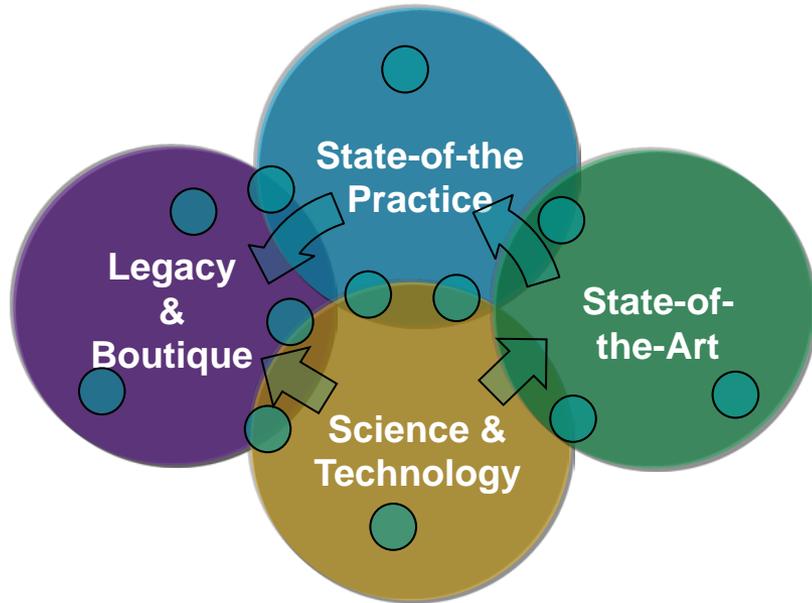
DoD MINSEC

- Next generation R&D DARPA (ERI) captured in US
- Modernization & assurance for DoD & nation through Innovation ecosystems
- Radiation hardened micro-electronics for nuclear and space

Domestic Foundry & Packaging

- Multiple competitive State-of-the-Art Foundries on shore
- Leadership in R&D and production
- Strong commercial business models
- Government business model for innovation & assurance

Trusted and Assured Microelectronics (T&AM) Domains and Technical Challenges



Availability

- Assured and expanded supply chain for specialized microelectronics for DoD systems
- Increased assurance and expanded supply options for Legacy parts

Access

- Lower barriers to safely access and develop advanced semiconductor-based systems to address new threats
- Robust design & validation tool access

Assurance

- Leverage an assured global supply and partners in U.S. semiconductor industry
- Competitive advantage for new markets through enhanced assurance practices

ASIC

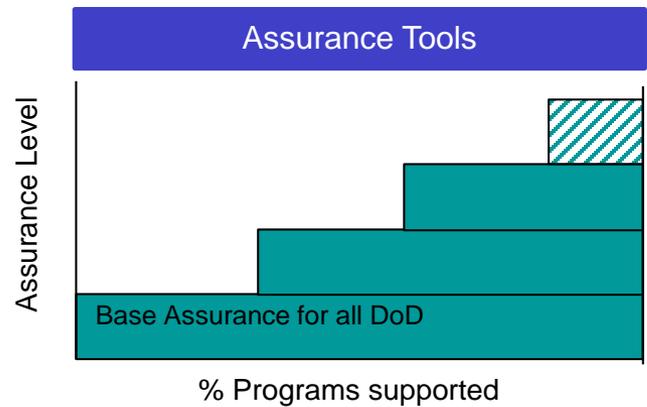
- Dense Digital CMOS
- RF & Mixed Signal
- Compound Semiconductors

FPGA

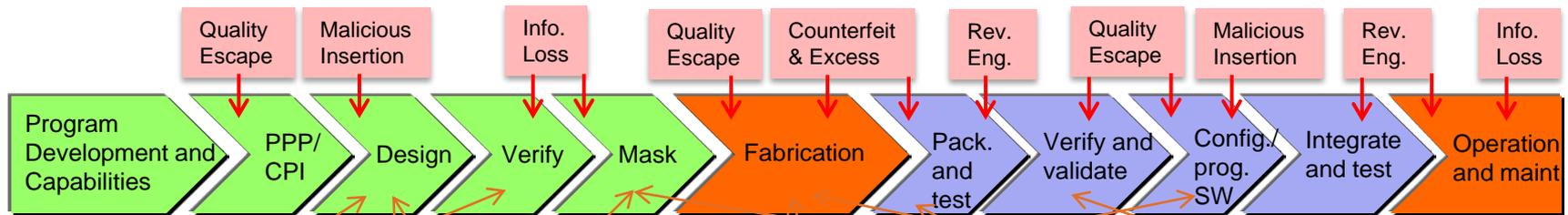
- Commercial SoC w/FGPA
- Rad-hardened
- Low-power

COTS

- Microcontrollers
- Analog components
- PCB assemblies



T&AM New Trust and Assurance Approaches



Design for trust	IP protection	Low-volume/high-mix production	Electronic component markers	Imaging technologies and forensics
<ul style="list-style-type: none"> Designing techniques to limit full use/functionality to trusted operation 	<ul style="list-style-type: none"> Preventing exploitation, including control of use, concealment, reconfiguring, partitioning, or employment 	<ul style="list-style-type: none"> Innovative methods to permit cost-effective, Trusted and assured low volume manufacturing of state-of-the-art ICs 	<ul style="list-style-type: none"> Tagging/marking ICs and subassemblies to authenticate and track supply chain movements 	<ul style="list-style-type: none"> Advanced capabilities to efficiently evaluate dense, state-of-the-art commercial components

Implement and demonstrate assurance capability with transition partners

Joint Federated Assurance Center (JFAC)



- **Federation of DoD software and hardware assurance (SwA/HwA) capabilities and capacities**
 - Support programs in addressing current and emerging threats and vulnerabilities
 - Facilitate collaboration across the Department and throughout the lifecycle of acquisition programs
 - Maximize use of available resources
 - Assess and recommend capability and capacity gaps to resource
- **Innovation of SW and HW inspection, detection, analysis, risk assessment, and remediation tools and techniques to mitigate risk of malicious insertion**
 - R&D is key component of JFAC operations
 - Focus on improving tools, techniques, and procedures for SwA and HwA to support programs
- **Federated Organizations**
 - Army, Navy, Air Force, National Security Agency (NSA), Defense MicroElectronics Activity (DMEA), Defense Information Systems Agency (DISA), National Reconnaissance Office (NRO), and Missile Defense Agency (MDA) laboratories and engineering support organizations; Intelligence Community and Department of Energy

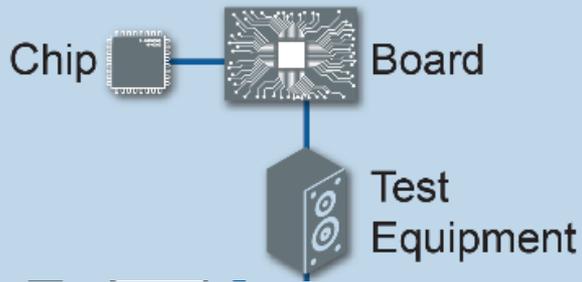
Portal: <https://jfac.navy.mil>

JFAC mission is to support programs with SwA and HwA needs

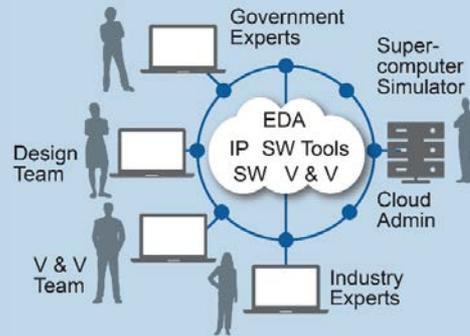
T&AM Program Focus Areas



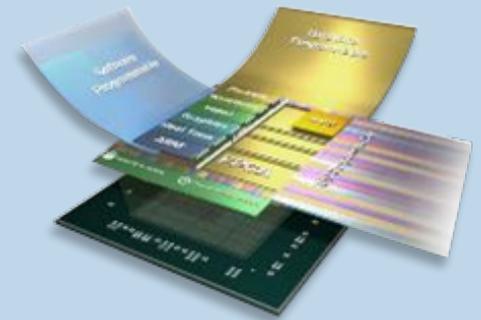
Verification & Validation



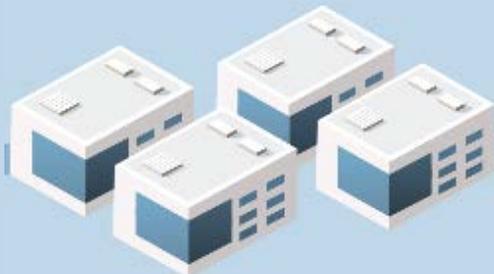
Design Assurance



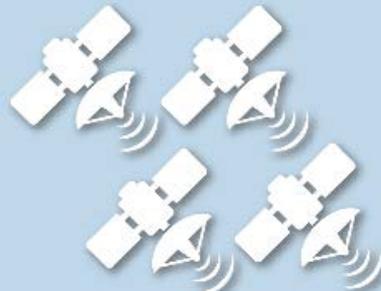
FPGA Assurance



Enhanced Manufacturing



Rad-Hard Microelectronics



Outreach & Standards



Microelectronics Trust Verification Technologies



- **Verification needed when Trusted Foundry not available**
 - DoD formed JFAC to provide this service
 - Long-term challenge to analyze leading-edge ICs and scale up capacity

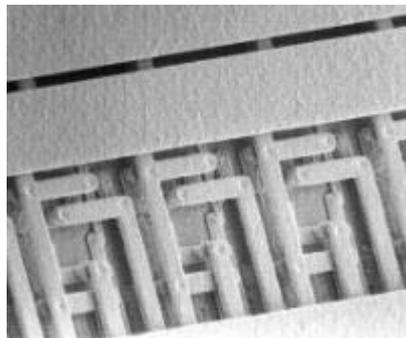
Design Verification

- Verification/assurance of designs, IP, netlists, bit-streams, firmware, etc.



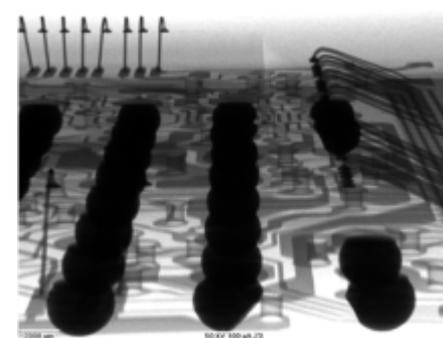
Physical Verification

- Destructive analysis of ICs and Printed Circuit Boards



Functional Verification

- Non-destructive screening and verification of select ICs

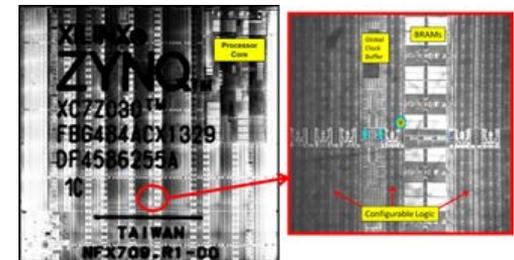
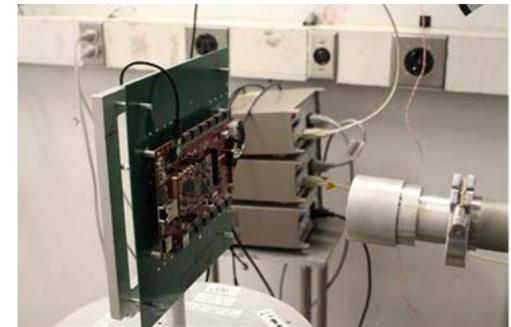


DoD, Intelligence Community, and DoE enhancing capability to meet future demand

Verification and Validation Accomplishments



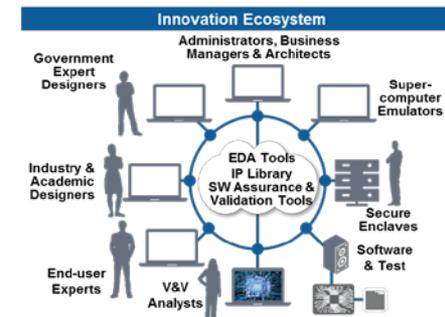
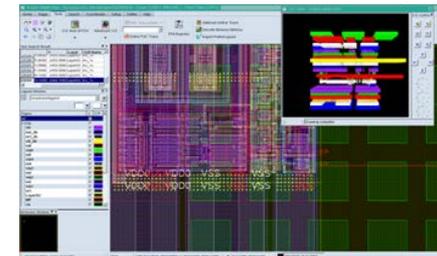
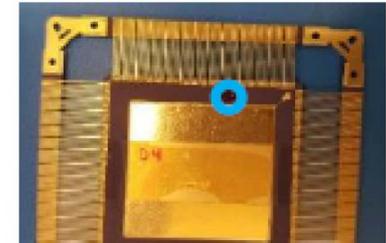
- Hardware Analysis Tool Suite, completed and distributed to JFAC core labs
- Demonstrated die de-processing and imaging of a device, including transistor and metal layers
- Developed methodology for security review of an untrusted, third-party communication network protocol.
- Physical and Functional V&V in support of DoD Programs
- Supply Chain Illumination support to DoD Programs



Design Assurance Accomplishments



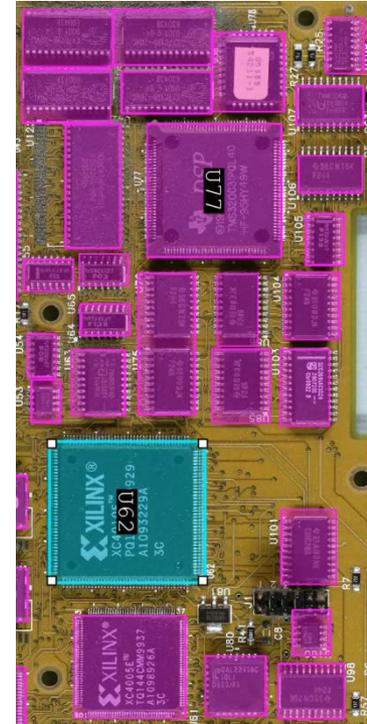
- Successfully demonstrated proof of operation for embedded dielet, which allows new microelectronics to be tracked through the supply chain
- Established state-of-the-art design capabilities that provide DoD programs with the same capacity and capabilities as commercial design teams
- Developed the Trusted-Silicon Stratus (TSS) Distributed Transition Environment (DTE) for hosting design tools, verification tools, and new IP, which will contribute to increased assurance in new DoD systems



Field-Programmable Gate Array (FPGA) Assurance Accomplishments



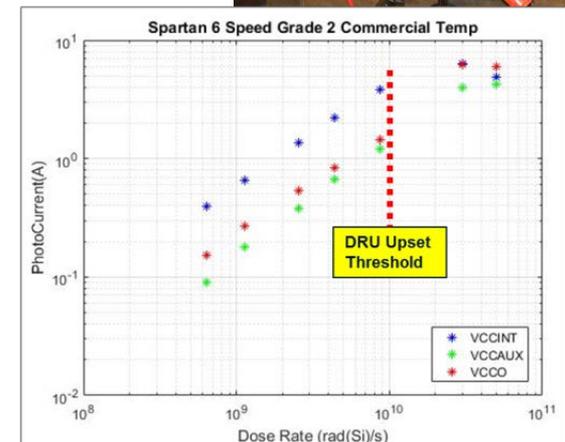
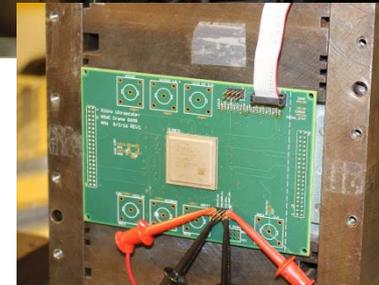
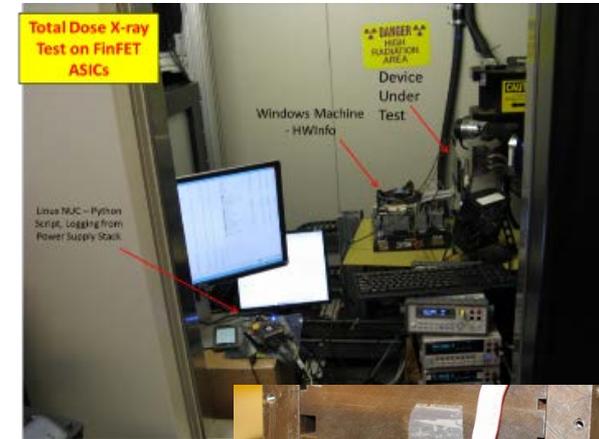
- Performed supply chain analysis for several FPGAs
- Developed hardware assurance standard operating procedure
- Formed supply chain sub-group to foster stakeholder collaboration
- Completed survey of FPGA and programmable logic device usage across DoD programs



Radiation-Hardened Microelectronics Accomplishments



- Performed radiation dose tests on state-of-the-art ASICs
- Tested COTS FPGA-supporting non-volatile memories for radiation hardness
- Established Strategic Radiation Hardened Electronics Council (SRHEC) to oversee requirements and issues across the government
- Surveying foundries for analog circuit radiation hardened production capabilities





Microelectronics Innovation for National Security and Economic Competitiveness (MINSEC)



Strategic National Security Applications



Secure IoT



Financial & Data Analytics



Autonomous Systems + AI



Robust + Agile Communicators



Commercial Space



Biomedical

Strategic National Economic Competitiveness Applications

Proactive Awareness & Security

- Supply Chain track
- Proactive Authorities
- Intelligence & CI
- Standards

Access & Assurance

- Secure Design
- IP, EDA, experts
- Foundry assured Access 
- Modernization & co-development

Enhanced Manufacturing

- SOTP Back-end parity with SOTA
- SOTA on 200mm tools at SOTP
- High-mix low vol. fabrication

Incentives & Market Growth

- Acquisition reform and incentives
- Tax, policy, regulation reform
- R&D and domestic fab incentives

Strategic Alliances

- Cooperative R&D
- Trade and Foreign Military Sales (FMS)
- Americas
- Europe
- Asia partners

Disruptive Research & Development

Experts, Infrastructure, Innovation, Venture Capital, Industrial Base, Academia

DoD MINSEC Highlights



R&D & Security

Develop the Next Generation Technology
DARPA Electronic Resurgence Initiative R&D Programs with matching from industry

Capture & Secure R&D in US Ecosystem
Secure design environments, foundry access and enhancement, security support

Modernization & Security

New Capability Development w/ Assurance & Insertion into DoD, dual use products (1000x COTS)

Assured COTS Programmable Co-Development

Obsolescence & Replacement

Workforce Development

Specialty Needs

Rad-Hard Microelectronics
Deliver future nuclear and space modernization

RF & Optical Technologies
Deliver unique RF and optical technologies for DoD systems

\$2.2B FY19-23 Results & Deliverables

Materials

Devices

DARPA ERI

Design tools

Architectures

Secure design environments

Intelligence & counter intelligence

Domestic enhanced R&D fabs

Most Advanced Digital Imagers

EW Array SoC

Secure PNT SoC

EW resistant

Assured FPGA from 2 vendors

ML/AI SoC

**2 Chips = 8 Peta FLOPS
400,000 FPS,
240W**

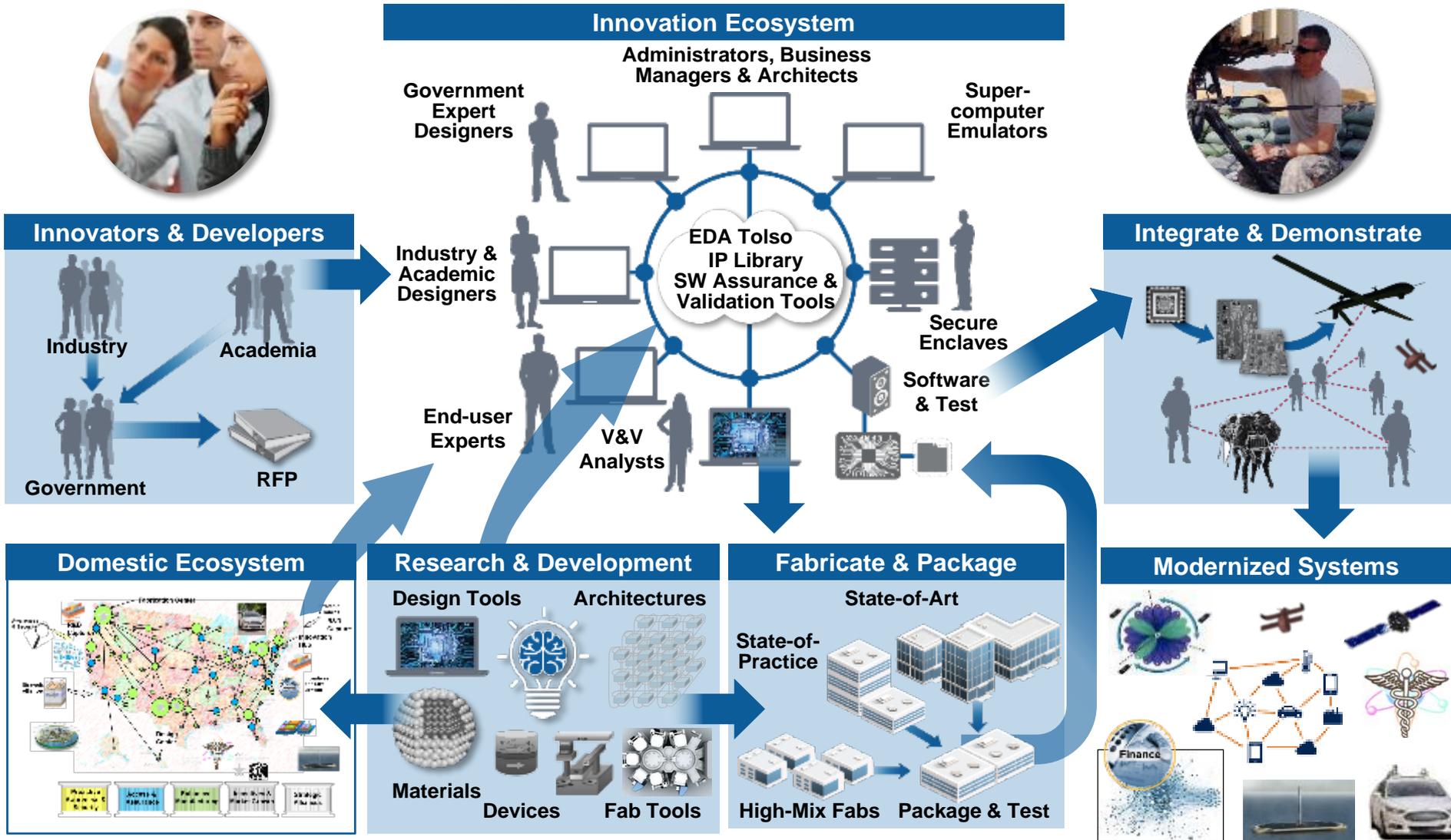
10k X GPU

Preserve access to legacy IP and processes
Future obsolescence replacement of boards by SoCs

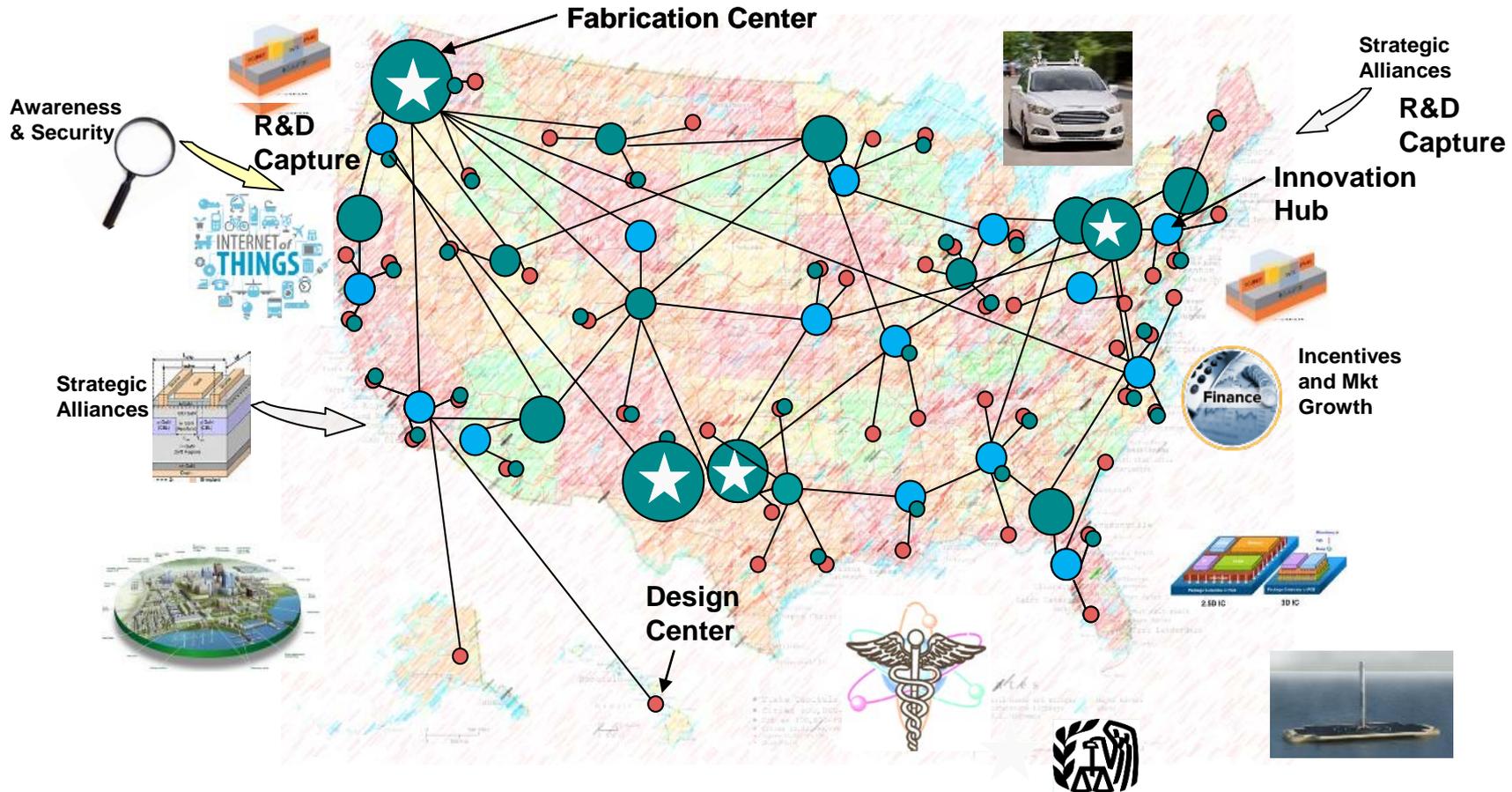
100 STEM scholarships including microelectronics specialization

- Domestic USG fab enhanced from 90nm AL to 65nm copper back-end process developed in partnership with NNSA
- Rad-hard by design developed for 1-2 SOTA foundry offerings with limited testing and qualification (strat-RH)
- Secure design and development of radio frequency and optoelectronic IP and test articles
- JFAC and NSA evaluation and qualification using SOTP and SOTA foundries

New Capability Development Operational View



Create Microelectronics Innovation Throughout the United States



Teaming and Partnerships Are Key to Success



- Many stakeholders are involved in the success of the long-term strategy:
 - Leadership from OSD, Services, and Agencies
 - Performers including Services, DMEA, DARPA, IARPA and other S&T organizations and laboratories
 - Integration and support of functions of:
 - DoD Trusted Foundry Program
 - DMEA Trusted Supplier Accreditation Program
 - Joint Federated Assurance Center
 - Microelectronics Assurance S&T and transition activities
 - Building and leveraging partnerships with Defense and commercial industry and academia for National Security and Economic Competitiveness
 - Coordination with other U.S. Government agency partners
- **Overall Bottom Line – structuring activities to meet acquisition program needs for trust and access to state-of-the-art microelectronics**

DoD Research and Engineering Enterprise

Solving Problems Today – Designing Solutions for Tomorrow



DoD Research and Engineering Enterprise
<https://www.acq.osd.mil/chieftechнологist/>

Defense Innovation Marketplace
<https://defenseinnovationmarketplace.dtic.mil>

Twitter
[@DoDIInnovation](https://twitter.com/DoDIInnovation)

For Additional Information



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