



Survivability and Reliability of Silicon MEMS Components

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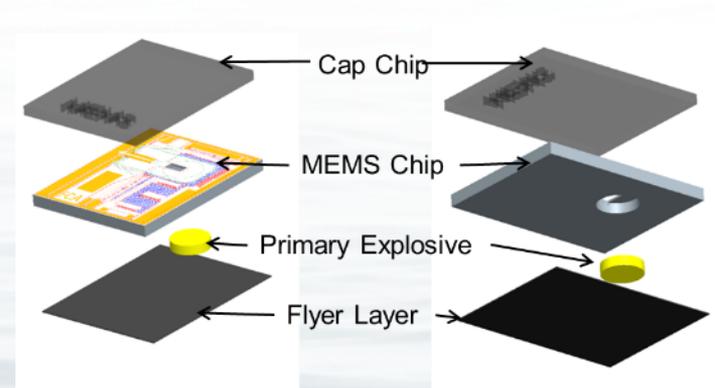
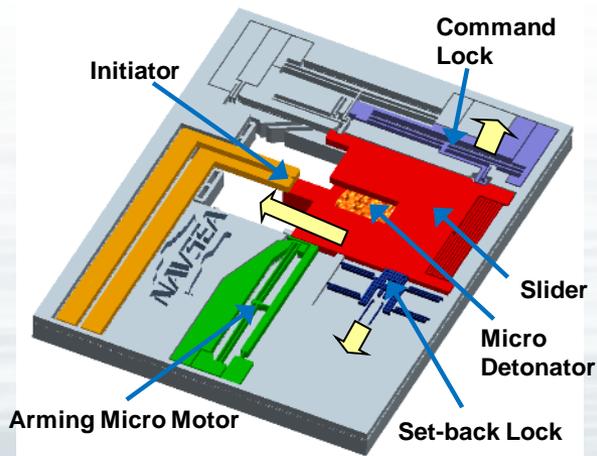
Capt. Scott H. Kraft, USN
Commanding Officer

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Technical Director

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MEMS Safe and Arm

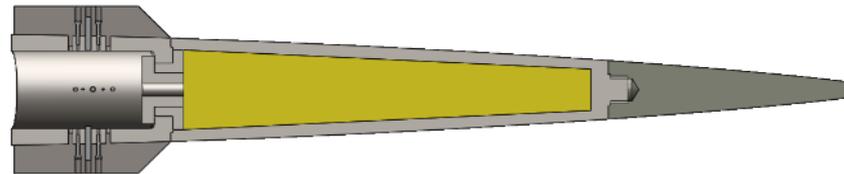
- Micro-electro Mechanical System (MEMS) Safe and Arm Devices (S&A) offer the potential for small volume, low cost, and low energy consumption.
- NSWC IHEODTD has nearly two decades of silicon/silicon on insulator (SOI) MEMS design, fabrication, and packaging experience.
- Safety locks: integrated mechanical structures used for command actuated locking architectures.
- Arming: design and fabrication of environmentally derived and command architectures.
- All non-explosive components fabricated on SOI wafers using established semiconductor processes.



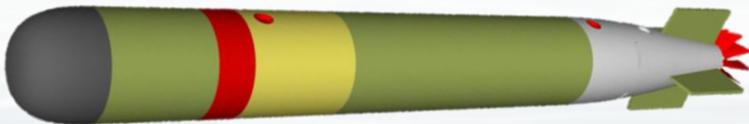


MEMS Fuzing Applications

Gun Launched Projectiles



Underwater Systems



Mortars

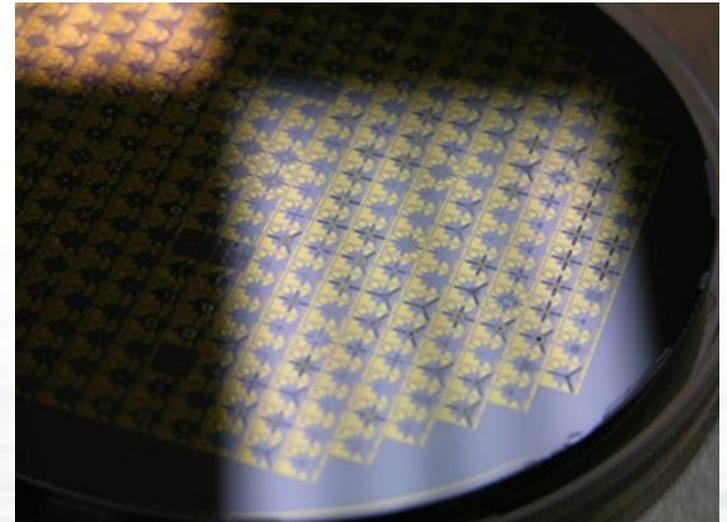




MEMS Reliability Description

Technology Goal: Assess the reliability of a microdetonator-based MEMS S&A by exposing multiple, packaged devices to simulated life cycle environments and performing subsequent failure identification and analysis in order to determine if it is capable of being utilized in a fuzing system that must meet a 99% reliability requirement.

Approach: Design, model, fabricate, and package MEMS S&A chips, expose the packages to environments determined by Mil-Std 331 and JOTP-052 that represent a fuze life cycle, assess any failures, and determine cause.



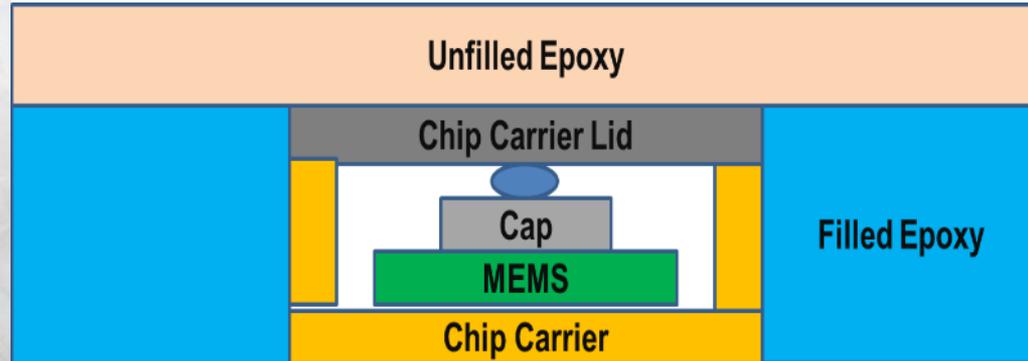
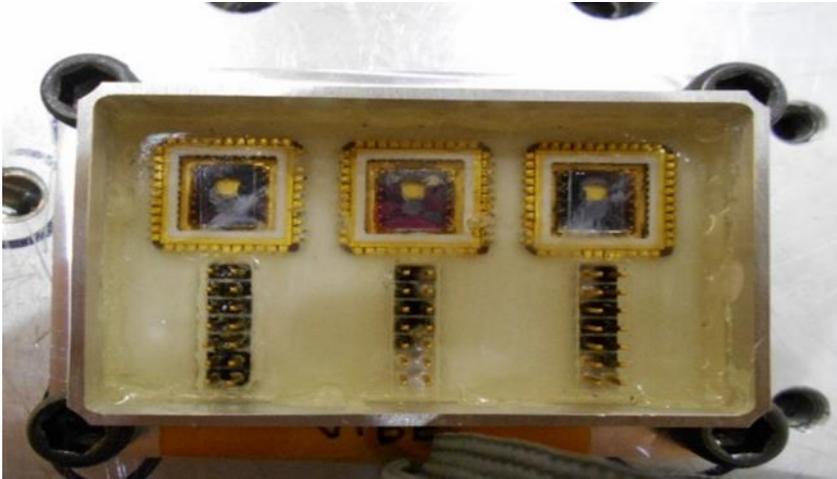
- Following work primarily funded under the Joint Fuze Technology Program



Test Matrix

Testing Purpose	Test	Results	Next Steps
Performance and Safety	T & H	Passed- No visual or electrical changes	Complete
Performance and Safety	Vibration	Passed- No visual or electrical changes	Complete
Safety	5 Foot Drop	On-going	Design and fabrication process refinements to improve subverted safety integrity
Performance	VHG	On-going	Inert and Live testing, final VHG tests will include the electronics board

Test Article Configuration



- 9 X 9 mm silicon MEMS S&A chip
 - Two of the three chips have a subverted lock (only one lock engaged)
- Wire bonded into a chip carrier (allowing for electrical interfaces through the electronics board below) for testing/functioning chip pre- and post-test
- Epoxy mixture with glass micro-balloons for shock absorption and clear mixture to allow visual inspection
- Aluminum housing fixture- represents a generic fuze housing



Temperature and Humidity Testing

Passed T&H Testing with No Adverse Effects to the MEMS

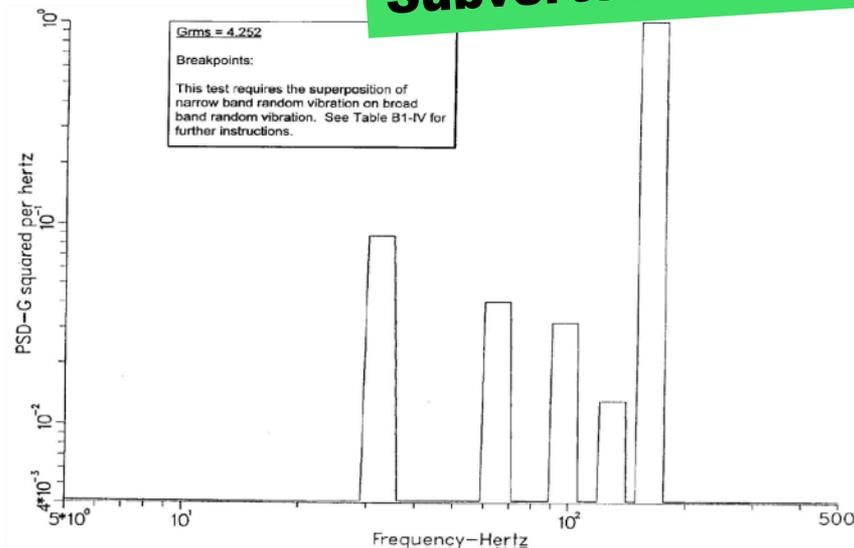
- Temperature/Humidity testing: Mil-Std 331-C appendix C, -54°C to 71°C and 95% humidity, cycling over 28 days
- Visually inspected MEMS and performed resistance checks pre- and post-tests
- Interesting note: unfilled epoxy (used in these tests for visual inspection) show cracks post test, while tactical micro-balloon filled epoxy seemed to be unaffected
- Johns Hopkins Applied Physics Laboratory: T&H Test Facility





Vibration Testing

Passed in Regular and Subverted Orientations



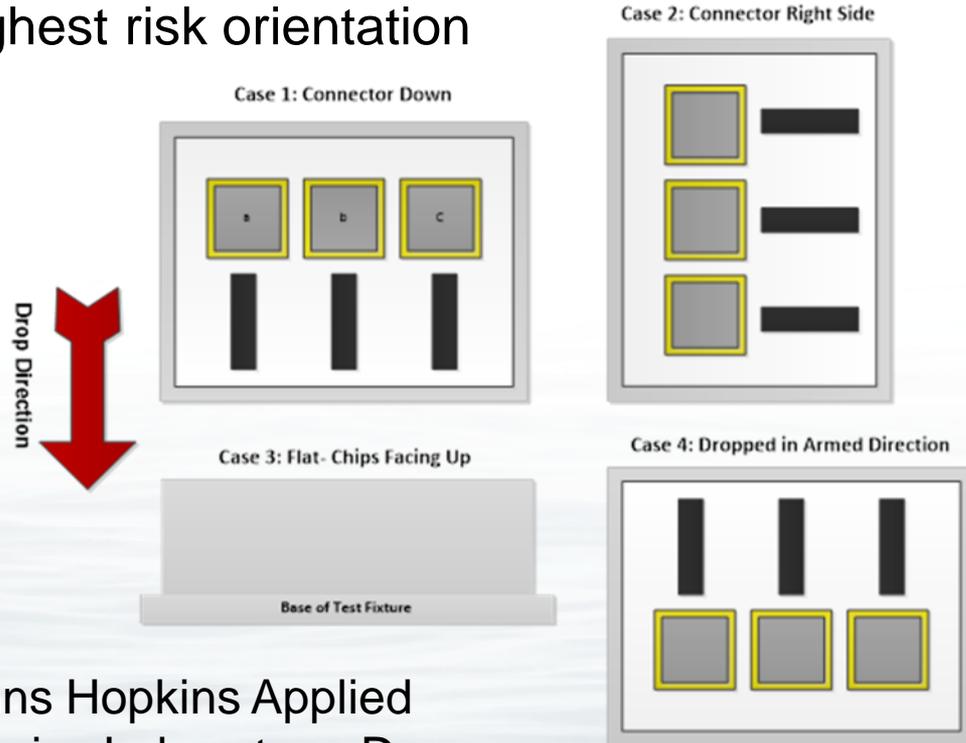
- Military tracked vehicle vibration determined to be harshest environment on MEMS S&A: Tests consisted of five phases ranging test levels from ~4-6 Grms
- Tested all five phases in X-, Y-, and Z- orientations with visual inspection and resistance checks pre- and post- testing
- Prior to test, locks were thickened to increase lock-slider interference which proved successful during these subverted tests
- Johns Hopkins Applied Physics Laboratory: Shaker Table

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Five Foot Drop Testing

- Pass criteria: Lock re-engages post-drop so slider is kept in safe position
- Previously passed dual-lock engagement drop tests, subverted chip testing to come
- Orientation where set-back lock latches out is highest risk orientation



- Johns Hopkins Applied Physics Laboratory: Drop Apparatus

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High-G Testing

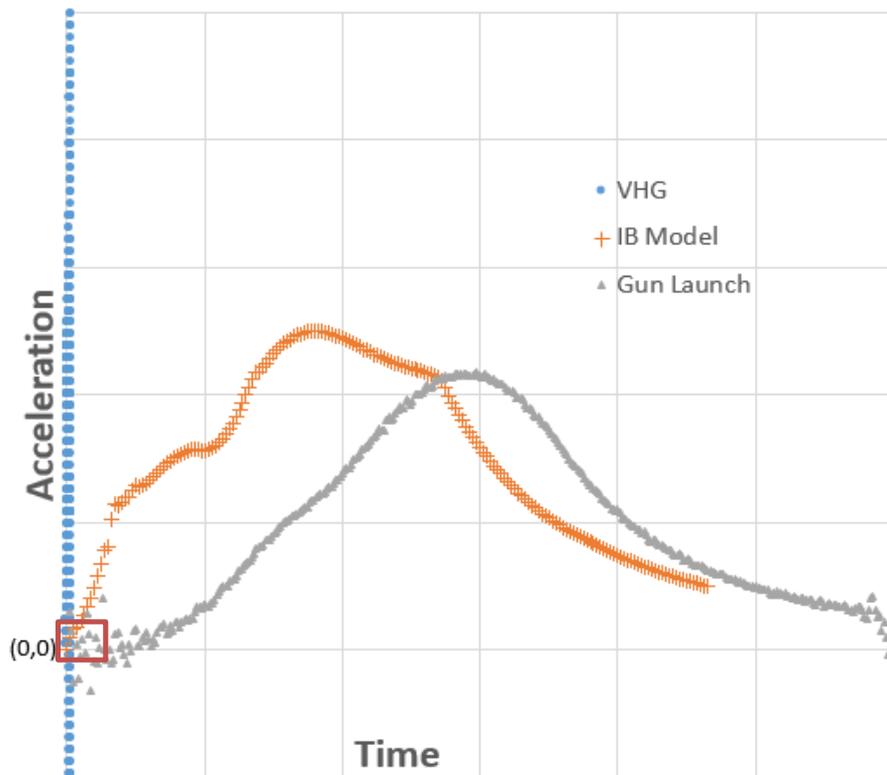


- Testing is on-going with efforts to minimize limitations and maximize the effectiveness of the tests
- Naval Surface Warfare Center Indian Head Explosive Ordnance Disposal Technology Division (NSWC IHEODTD): Very High-G (VHG) Machine

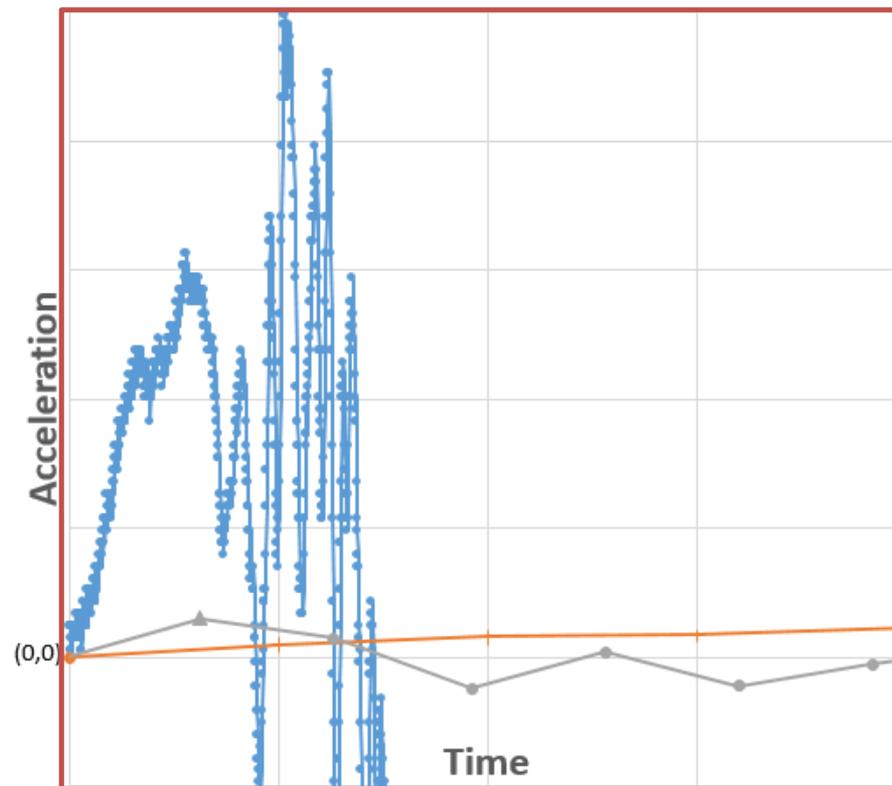


Comparison of Shock Impulses

Shock Level: Acceleration vs Time



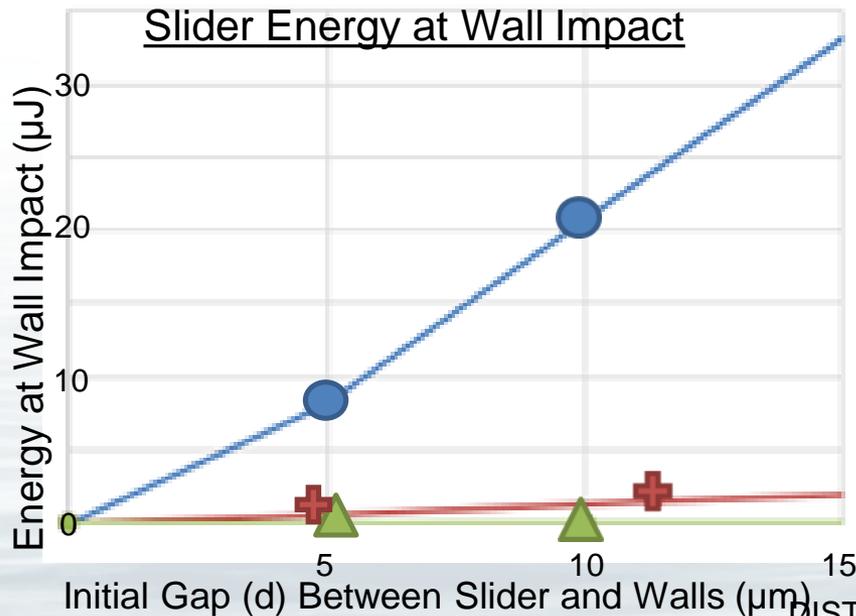
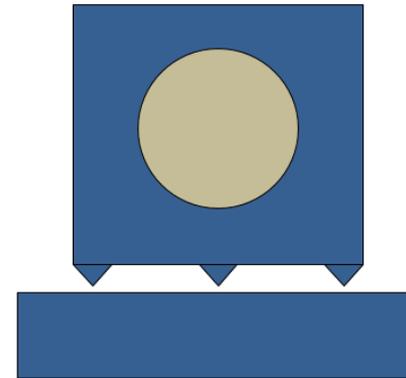
Zoomed in Shock Level Acceleration vs Time





High-G Testing

- Primary damage mechanism under inertial loading is from micro structure impact
- High ramp rate from VHG results in high relative velocities between micro-structures (over-test for slider)
 - Small clearance between guides (distance= key design parameter in decreasing impact velocities)
 - High ramp rate leads to high velocity impact
 - Lower ramp rate: gap is closed before peak acceleration is reached



Distance, d (µm)	VHG Energy (µJ)	Gun Launch Energy (µJ)	IB Model Energy (µJ)
0	0	0	0
5	8.06	0.54	0.04
10	20.76	1.51	0.11
25	57.91	3.41	0.04

- VHG
- Gun Launch
- IB Model

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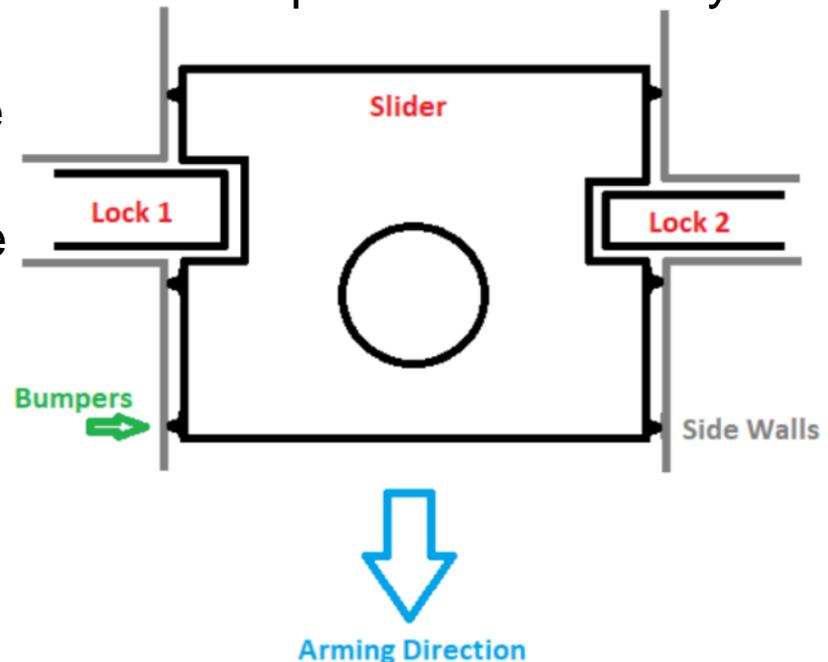
Upcoming Efforts

Drop Testing Efforts

- Conduct drop tests in various orientations with subverted chips

VHG Testing Efforts

- Refine the etching method for the slider bumpers to reduce the gap between bumpers from 30 μm to 10 μm to minimize slider impact damage.
 - Test chips with different gap sizes for comparison and theory validation.
- Refine VHG test methods to replicate damage modes of tactical shots
- Conduct VHG tests with inert and live MEMS S&A with updated testing procedures



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Conclusions

- Indian Head has been successful in T&H testing for MEMS S&A
- MEMS S&A chips have passed harsh vibration testing (tracked vehicle profiles)
- Tests are being conducted to prove MEMS S&A survivability for five foot drop
- Methods to more closely replicate gun launch shock profiles using VHG are being developed with upcoming inert and live tests to determine MEMS S&A high-G survivability



Questions?