



Sandia  
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ADVANCED  
FUZING  
TECHNOLOGY

# Effects of Orientation & Boundary Condition on Encapsulated Electronics

Presented By:

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[cwhite3@sandia.gov](mailto:cwhite3@sandia.gov)

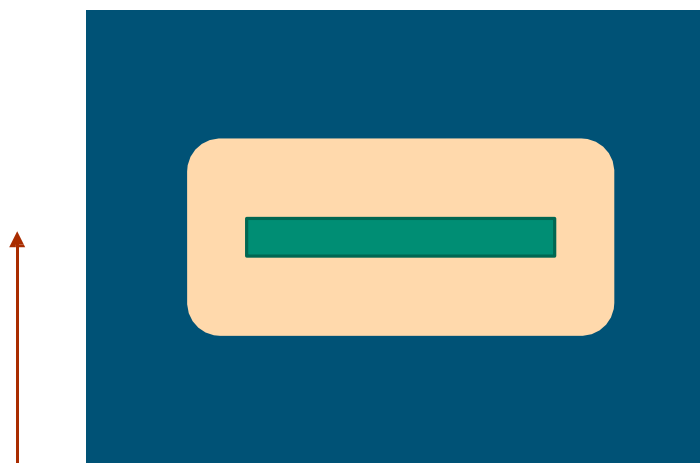
Distribution A/ Unclassified

SAND2021-5442 C

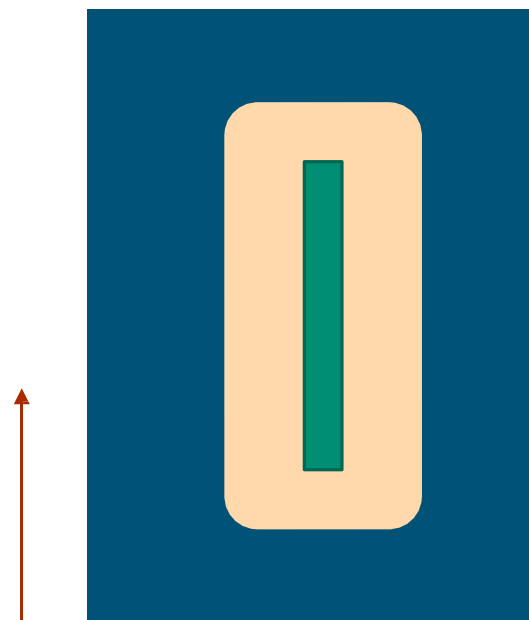




# Introduction



Horizontal / Perpendicular

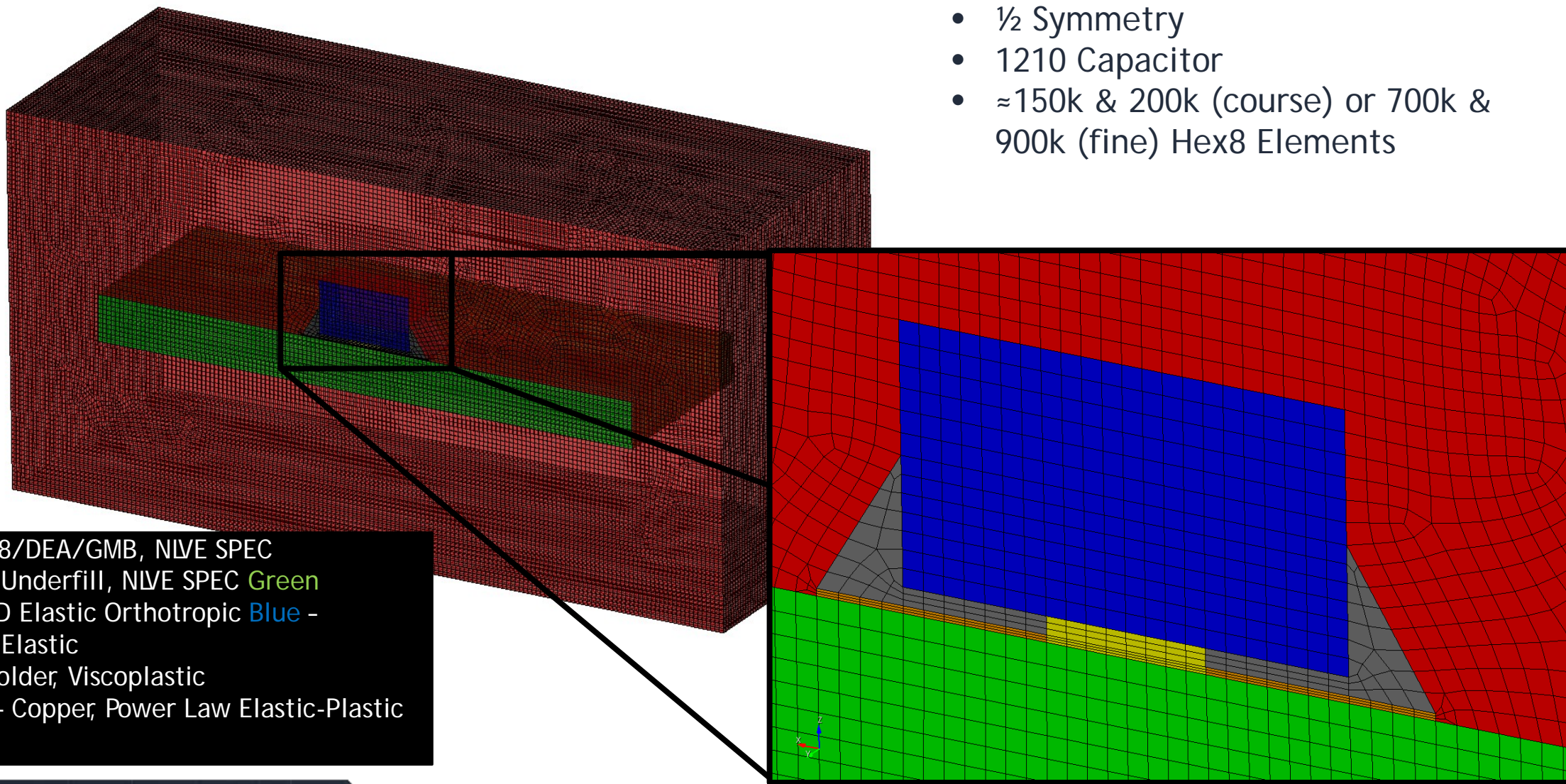


Vertical / Parallel



# Generic Mesh

- ½ Symmetry
- 1210 Capacitor
- ≈150k & 200k (course) or 700k & 900k (fine) Hex8 Elements

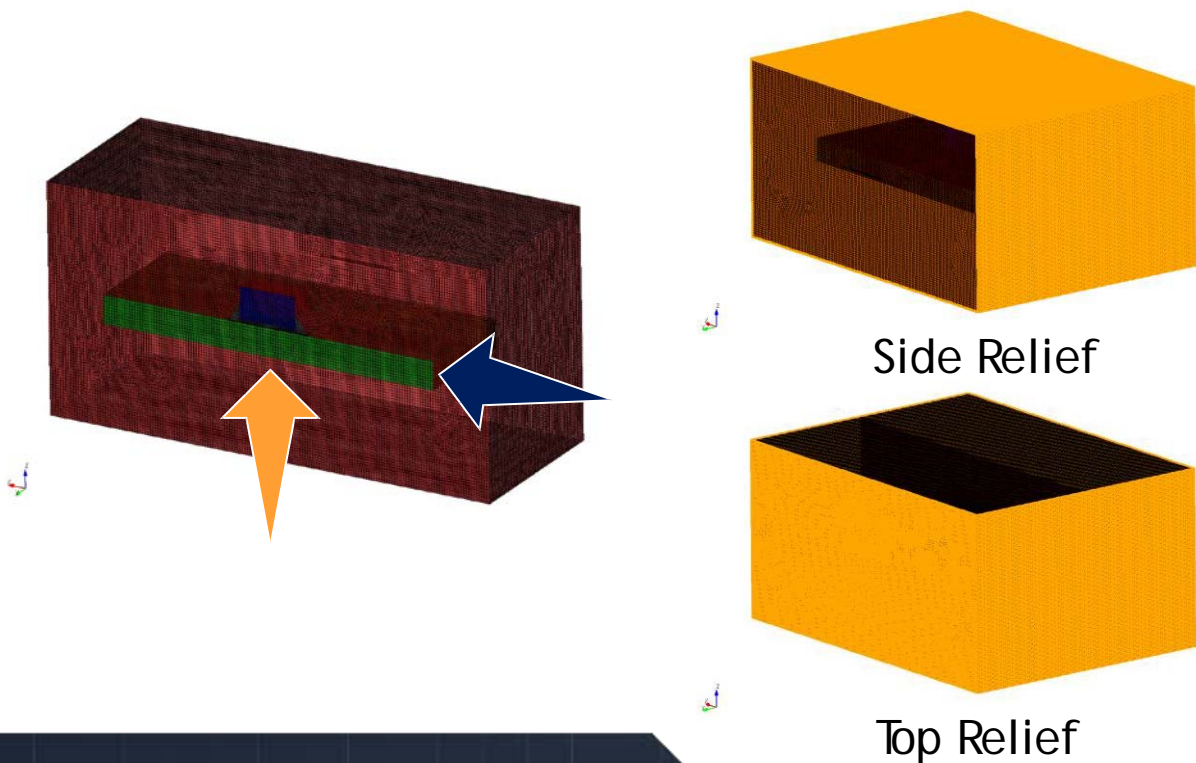


**Red** - 828/DEA/GMB, NIVE SPEC  
**Yellow** - Underfill, NIVE SPEC  
**Green** - FR4, 3D Elastic Orthotropic  
**Blue** - Ferrite, Elastic  
**Grey** - Solder, Viscoplastic  
**Orange** - Copper, Power Law Elastic-Plastic

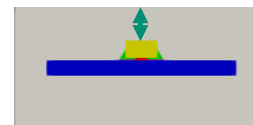


# FEA Procedure & Parameters

1. Instantiate parametric study with Dakota
2. Create generic mesh geometry using Cubit
3. Implicitly cure (Sierra/SM Adagio) from 70°C → 25°C
4. Explicitly accelerate (Sierra/SM Presto) fixed exterior with representative haversine pulse\*
5. Post-process with Python & Paraview



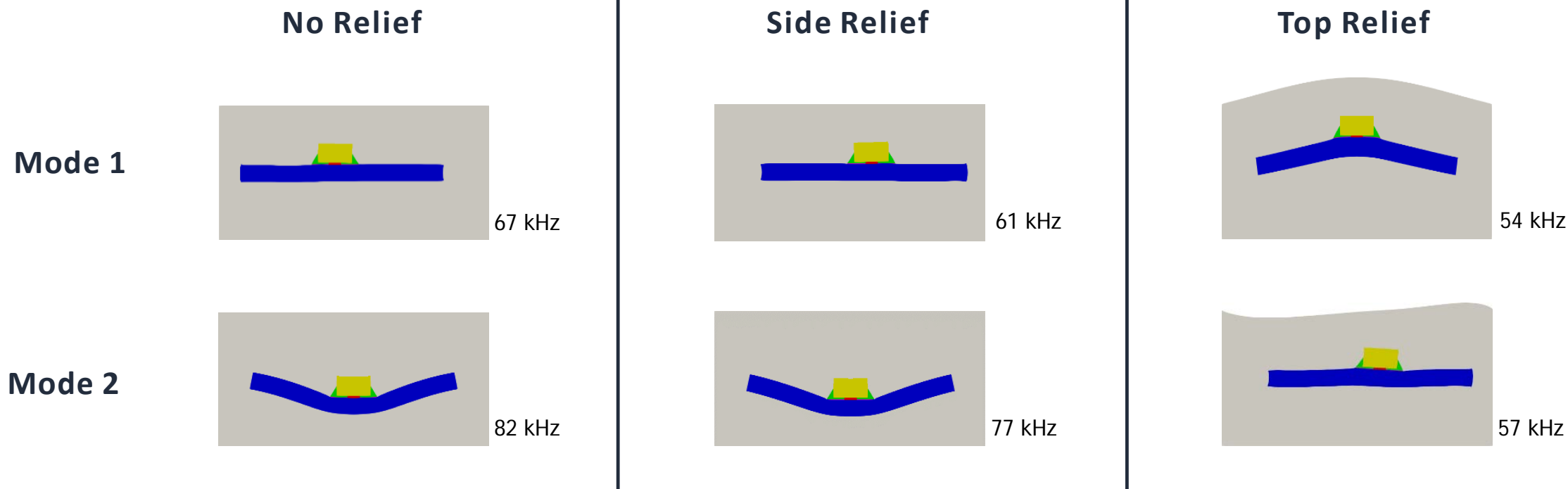
Parameter	Value
Boundary Condition	No Relief Side Relief Top Relief Bottom Relief Top/Bottom Relief
Loading Direction	Normal-to-PCB Parallel-to-PCB
PCB Length	.75"x.5"x.062" .50"x.5"x.062"
Boundary Proximity	.041" .075" .108" .141"
Mesh Size	Course: .010" Fine: .006"
Pulse Width (μs)	<u>1.95</u> , 2.93, <u>3.91</u> , 5.87, <u>7.81</u> , 11.72, <u>15.6</u> , 23.4, <u>31.3</u> , 46.95, <u>62.5</u> , 93.75, <u>125</u> , <u>250</u> , <u>500</u>



\*Simulation extended for 1 ms after pulse to allow assembly to freely resonate.

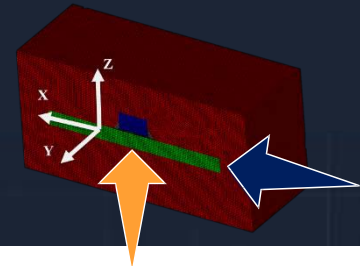


# Fundamental Mode Shapes

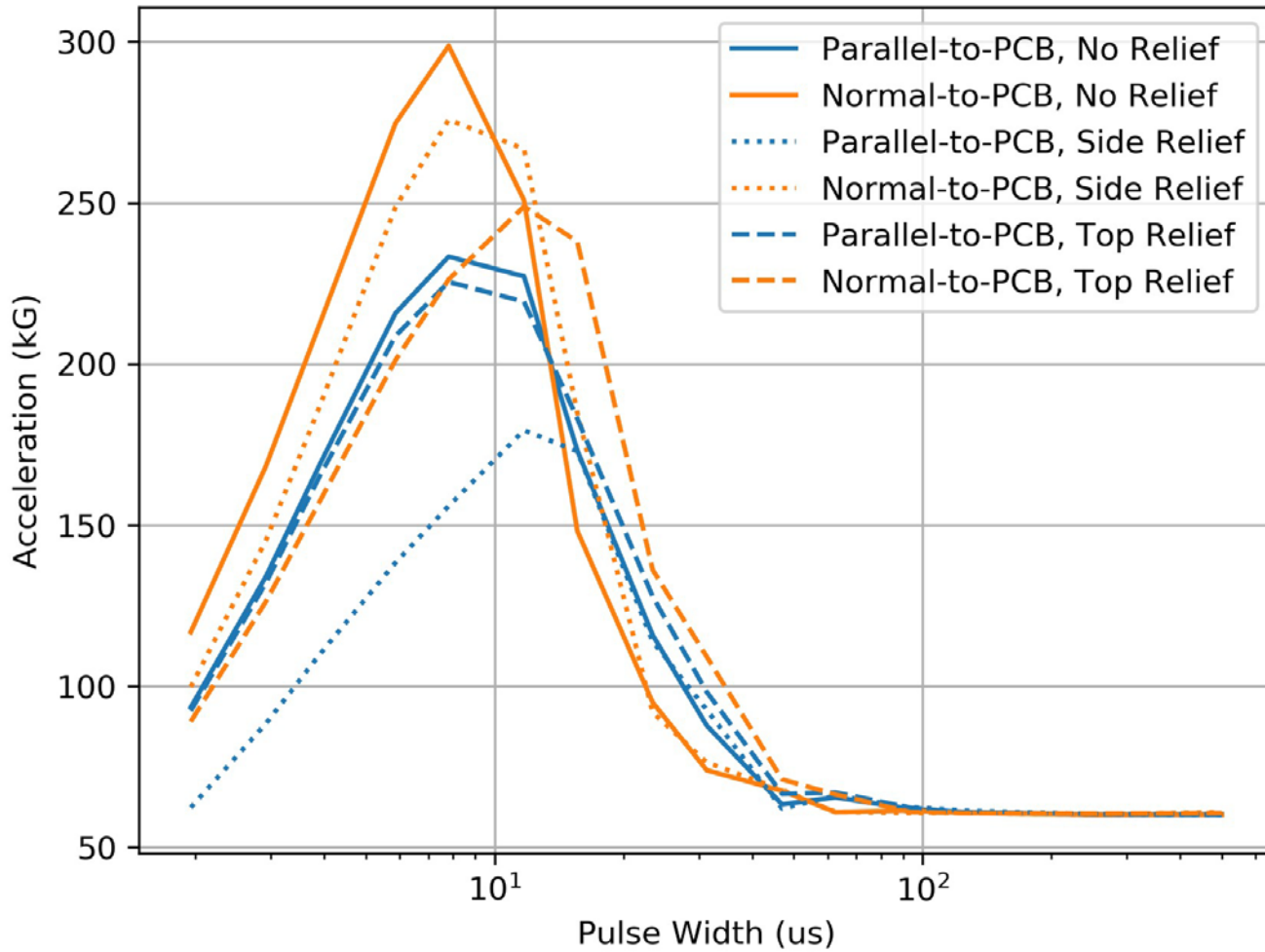


During mechanical insult, the shape of the PCB deflection is determined by the loading direction, regardless of boundary condition (i.e., different loading directions excite different modes).

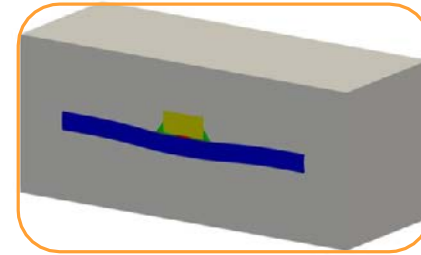
# Capacitor Acceleration Transmissibility



Peak Temporal, Spatial *Average*, Transmitted Acceleration

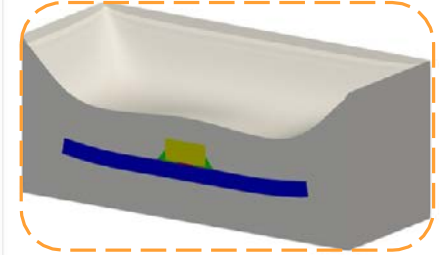


Normal-to-PCB  
No Relief  
(50X Mag)

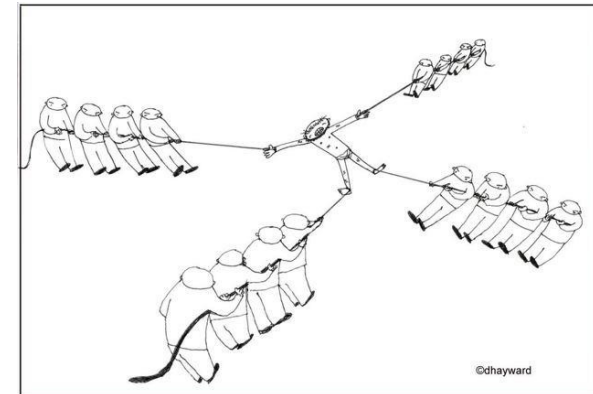


Time: 0.000020

Normal-to-PCB  
Top Relief  
(50X Mag)



Time: 0.000020

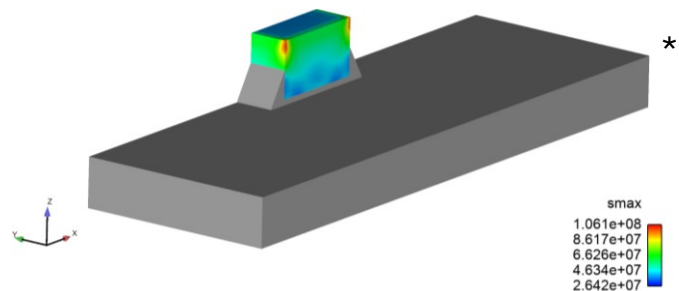
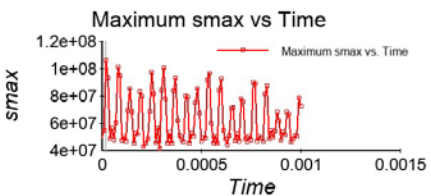
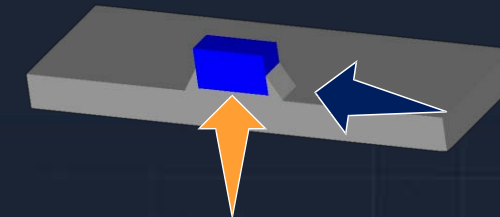


<http://clipart-library.com/images/ATbr5BAyc.jpg>

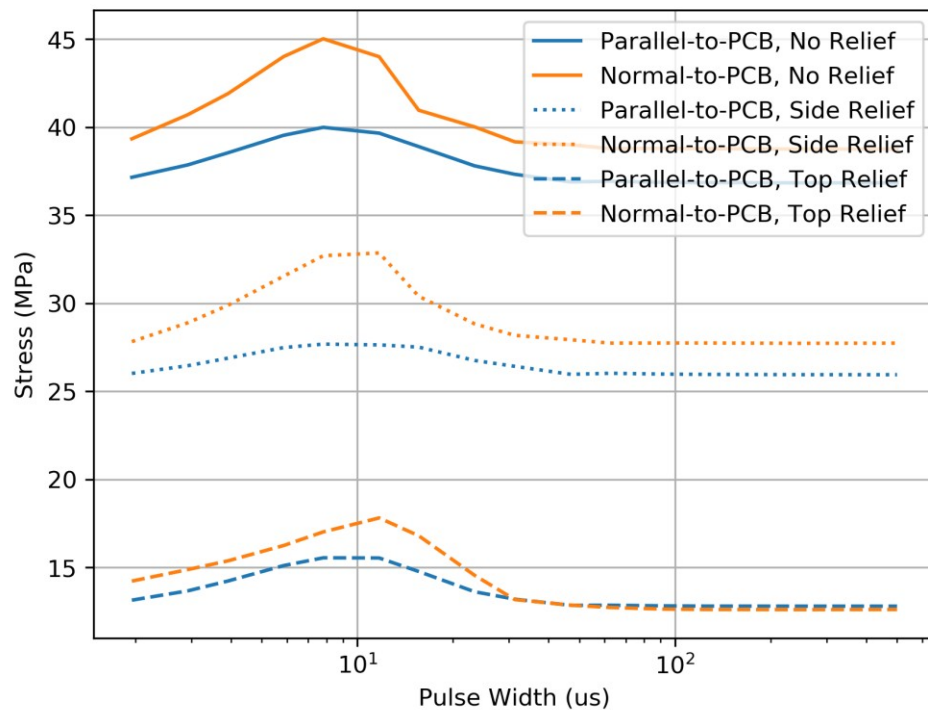
Relief mechanisms drastically affect deflection behavior.



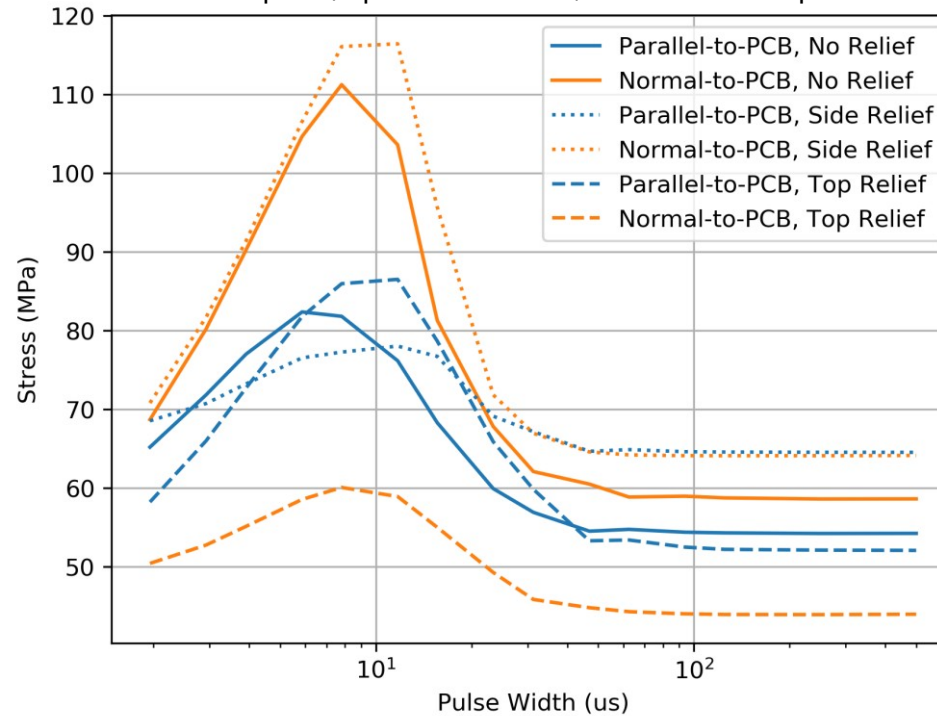
# Resultant Capacitor Stress



Peak Temporal, Spatial Average, Maximum Principal Stress



Peak Temporal, Spatial Maximum, Maximum Principal Stress

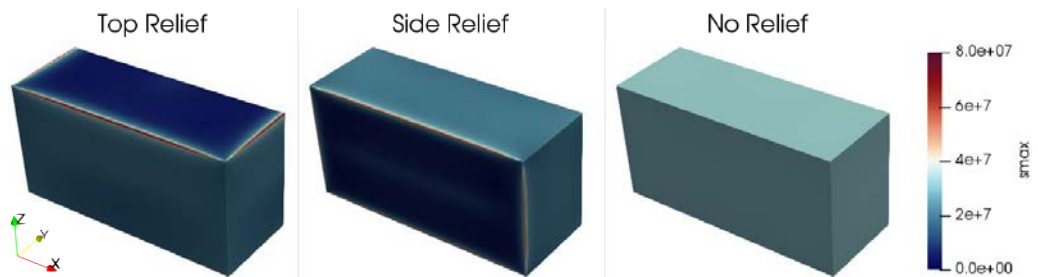
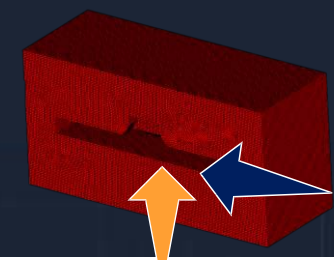


Tensile load on capacitor exacerbates dynamic stress.

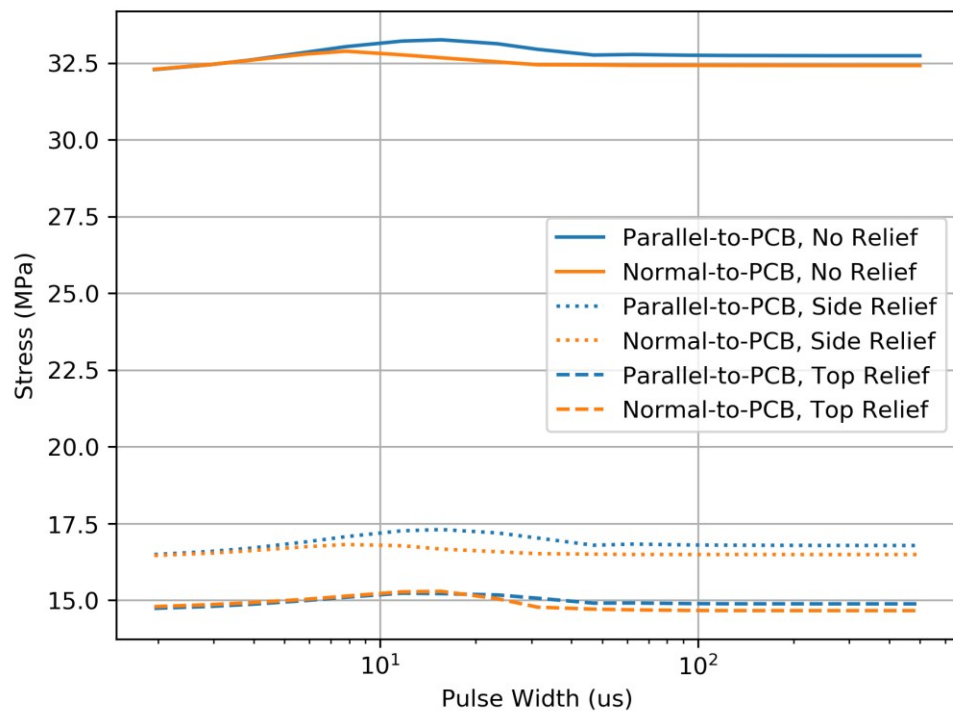
\*No Relief, Normal-to-PCB, Pulse Width: 7.81 μs



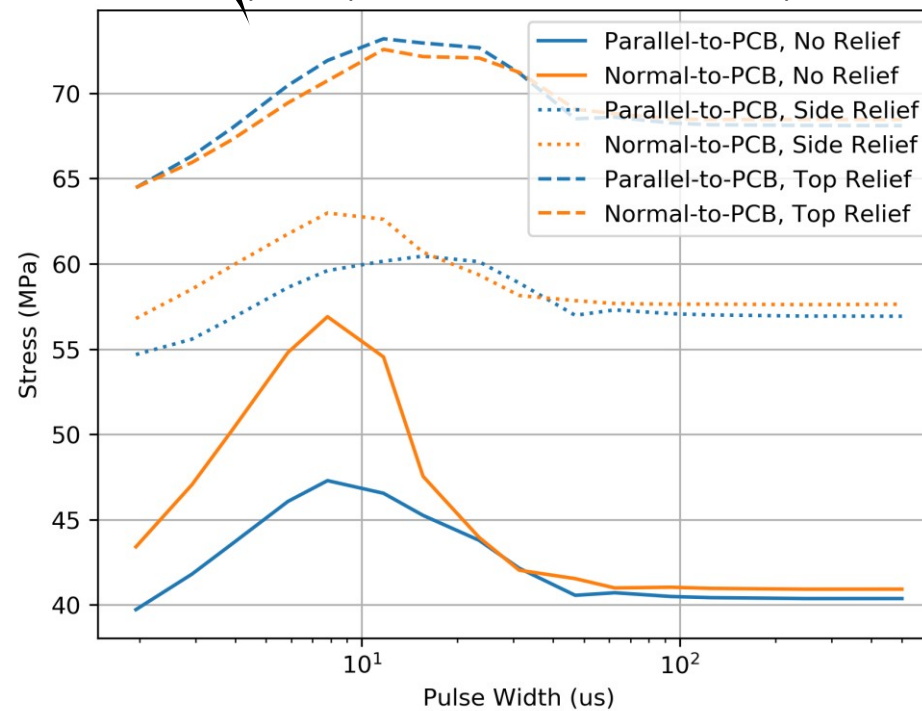
# Resultant Potting Stress



Peak Temporal, Spatial Average, Maximum Principal Stress



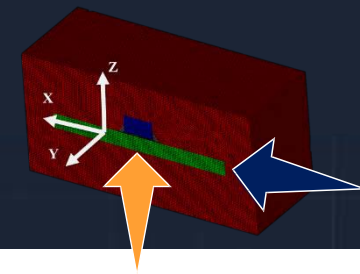
Peak Temporal, Spatial Maximum, Maximum Principal Stress



Delamination likely to occur along housing interface.

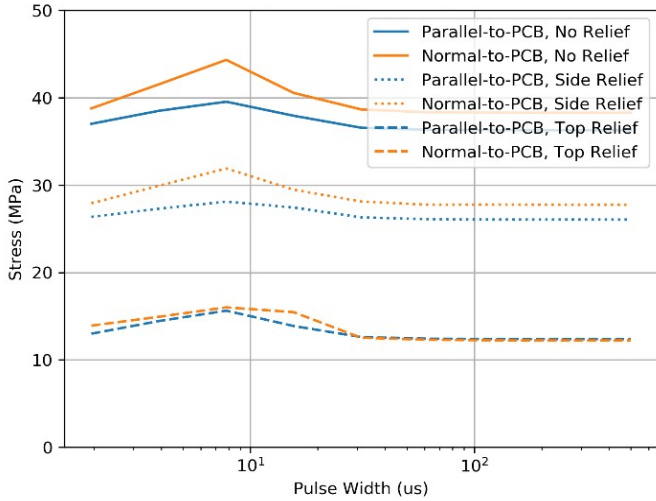


# PCB Length Comparison: Capacitor Stress



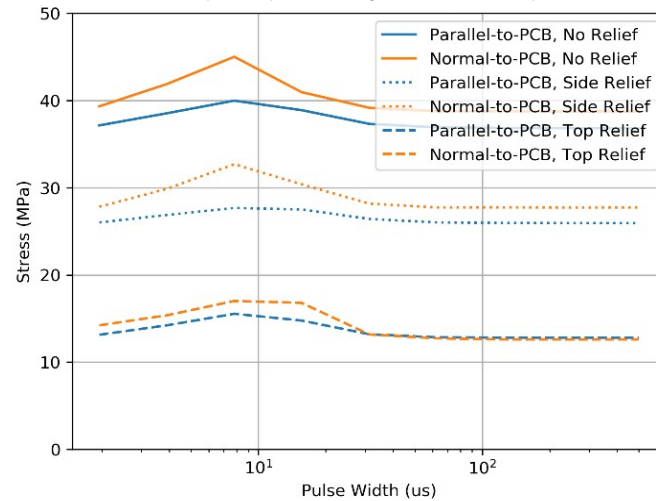
## .5" L PCB

Peak Temporal, Spatial Average, Maximum Principal Stress

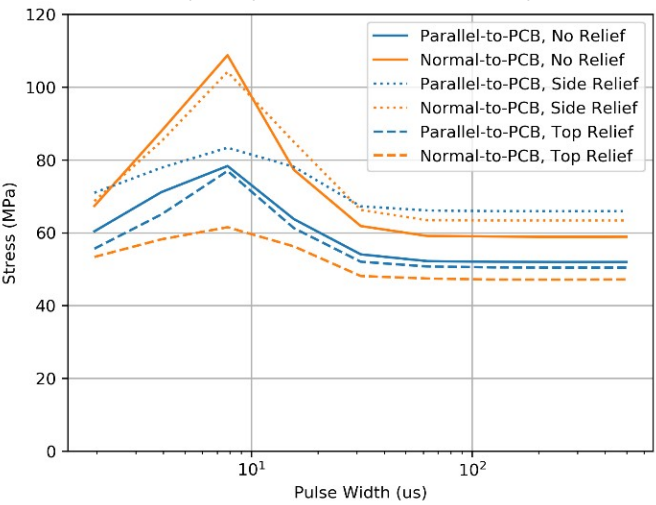


## .75" L PCB

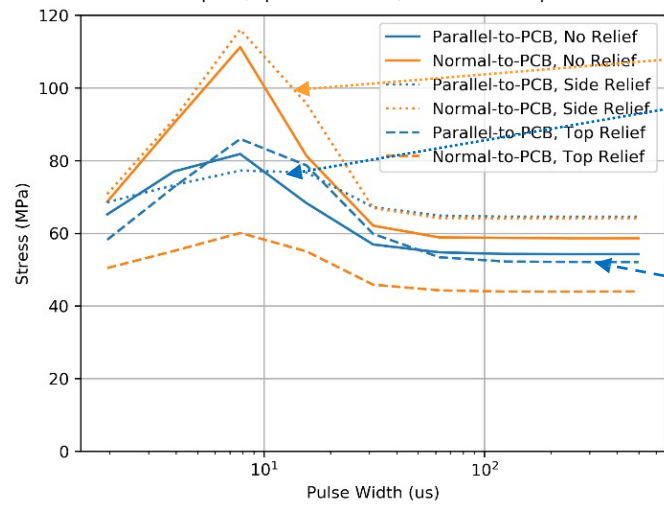
Peak Temporal, Spatial Average, Maximum Principal Stress



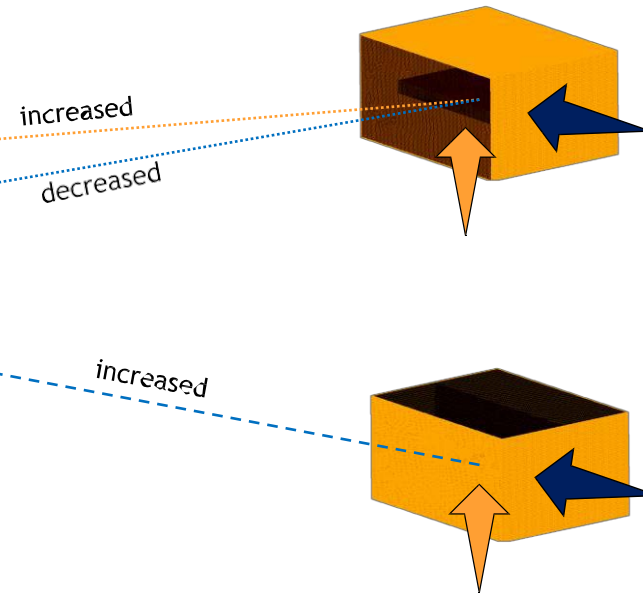
Peak Temporal, Spatial Maximum, Maximum Principal Stress



Peak Temporal, Spatial Maximum, Maximum Principal Stress

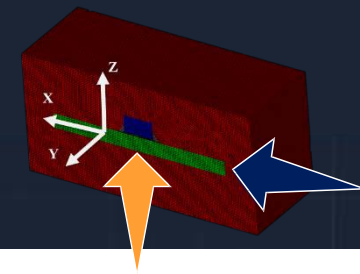


- Negligible effect on spatial averaged stress
- Stress increased for Normal-to-PCB/Side Relief and Parallel-to-PCB/Top Relief
- Stress decreased for Parallel-to-PCB/Side Relief



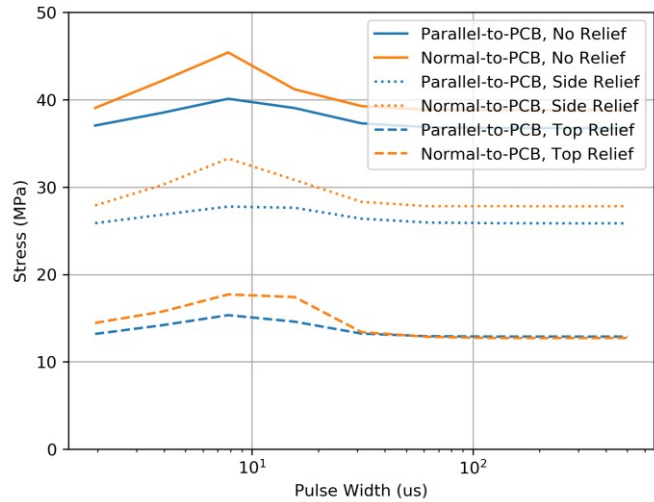
Increasing PCB length reduces bending stiffness and resonant frequency.

# Mesh Comparison: Capacitor Stress



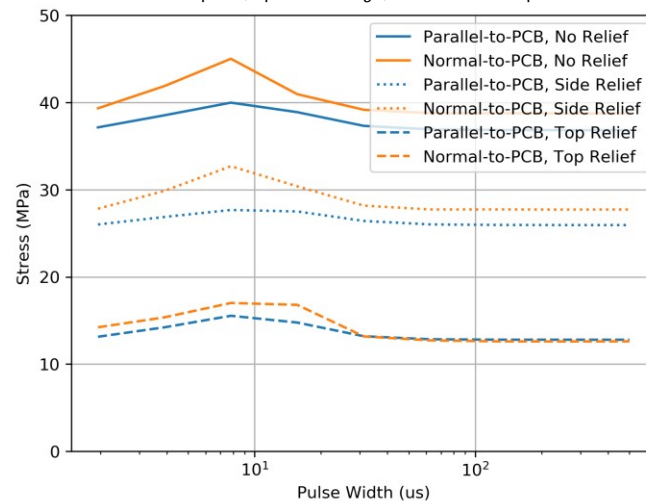
## Course: .010"

Peak Temporal, Spatial Average, Maximum Principal Stress

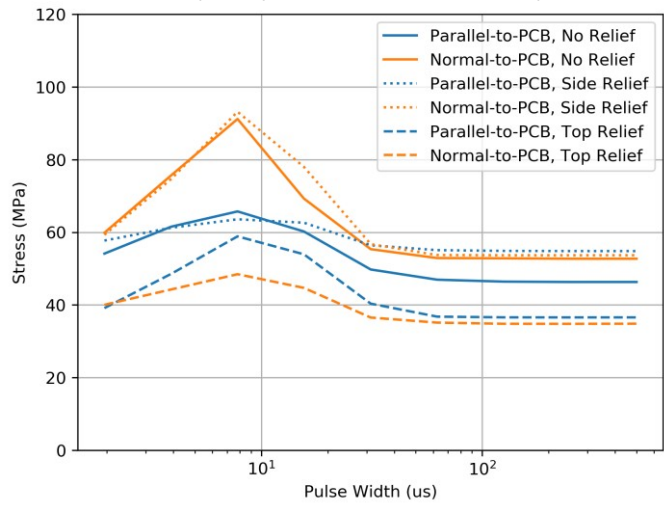


## Fine: .006"

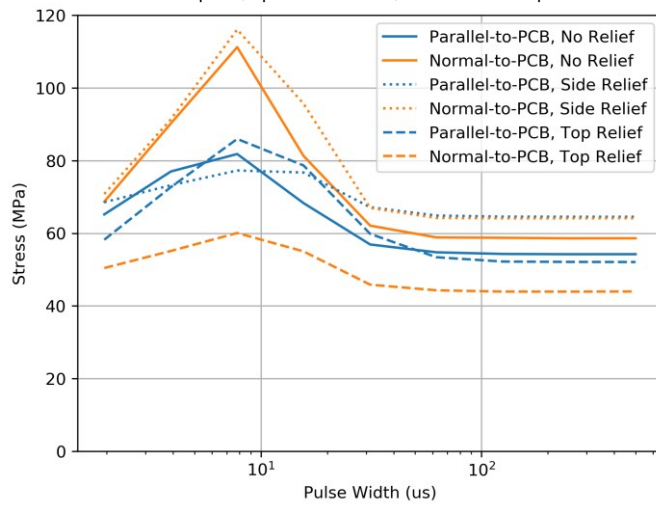
Peak Temporal, Spatial Average, Maximum Principal Stress



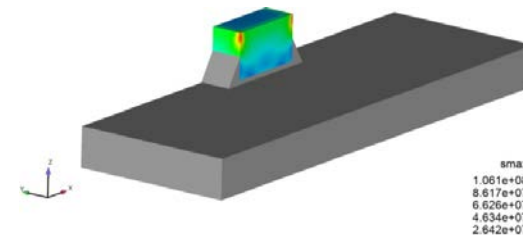
Peak Temporal, Spatial Maximum, Maximum Principal Stress



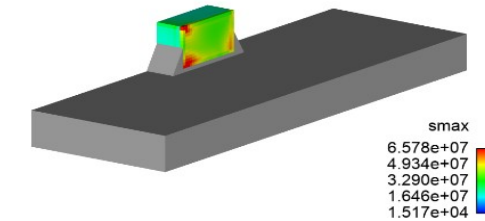
Peak Temporal, Spatial Maximum, Maximum Principal Stress



- Spatial averages stresses have converged
- Mesh contains stress risers which fail to converge



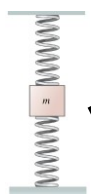
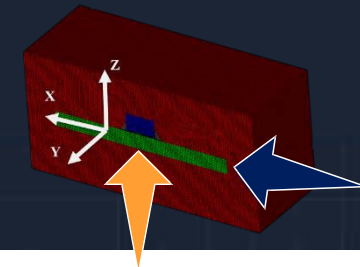
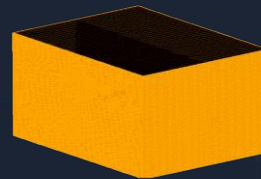
Normal-to-PCB/No Relief



Parallel-to-PCB/Side Relief

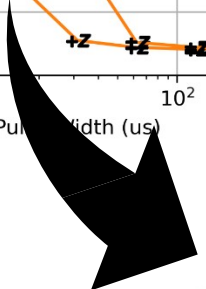
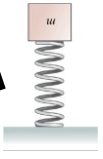
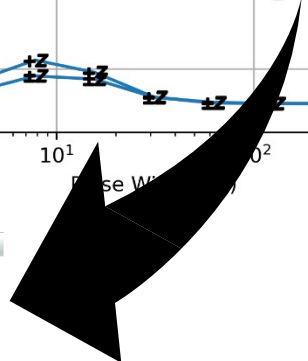
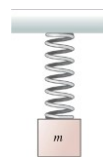
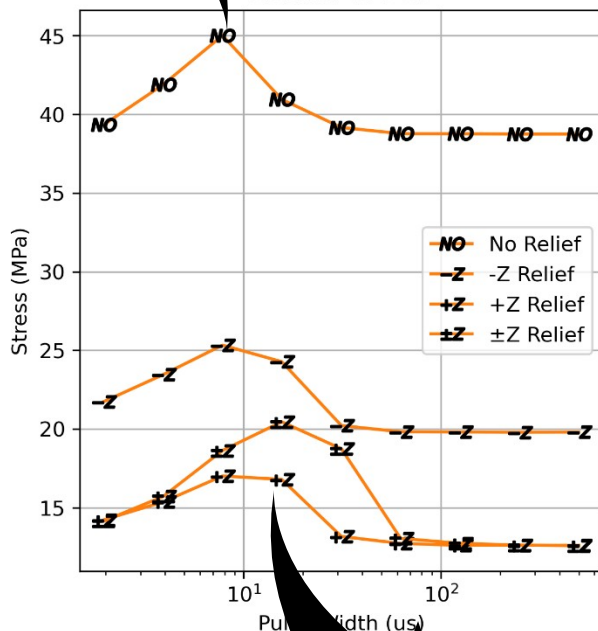
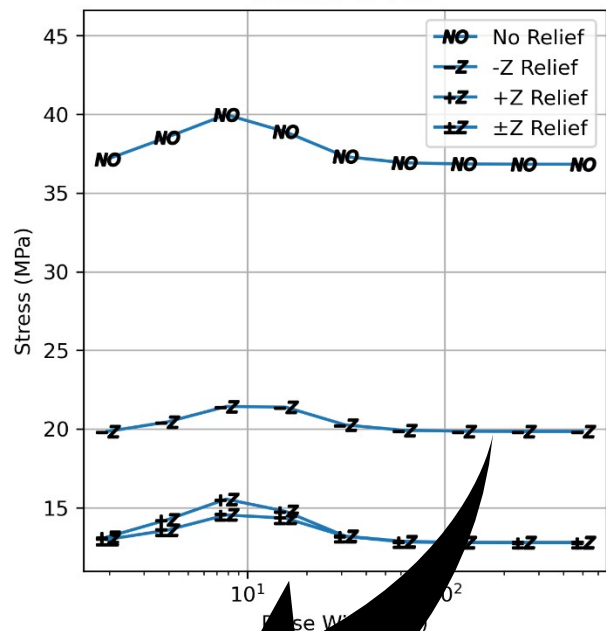
Geometry is mesh-dependent due to existence of stress concentrators.

# Bottom/Top Comparison: Capacitor Stress



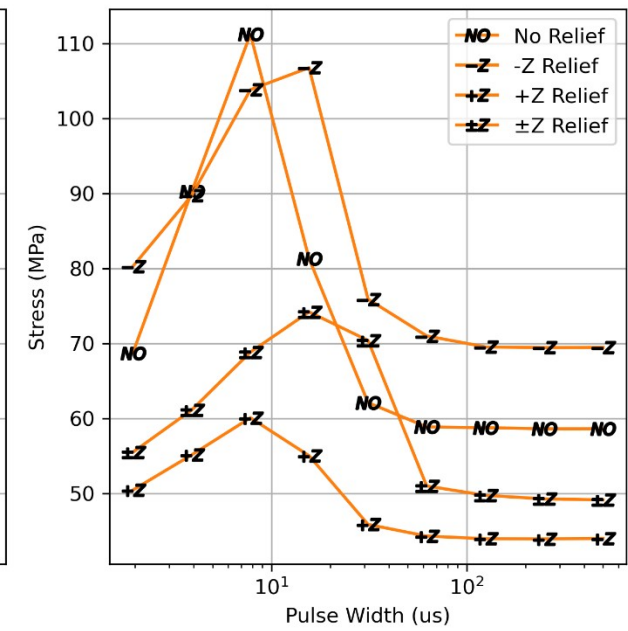
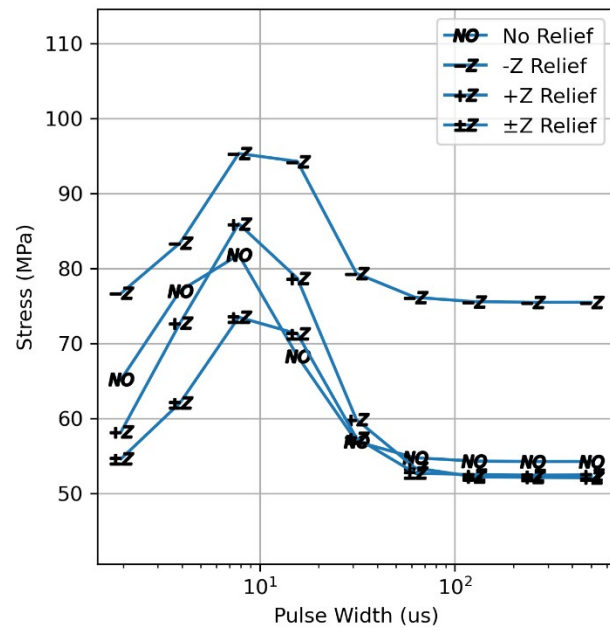
Peak Temporal, Spatial Average, Maximum Principal Stress  
Parallel-to-PCB

Normal-to-PCB



Peak Temporal, Spatial *Maximum*, Maximum Principal Stress  
Parallel-to-PCB

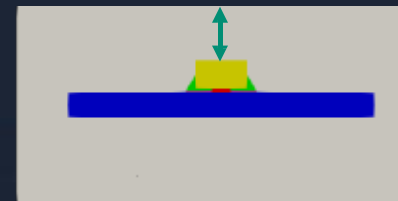
Normal-to-PCB



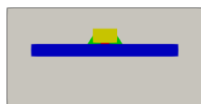
Tensile loads can resist PCB deflection; reliefs can exacerbate stress.



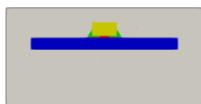
# Boundary Proximity: Average Capacitor Stress



0.141"



0.108"

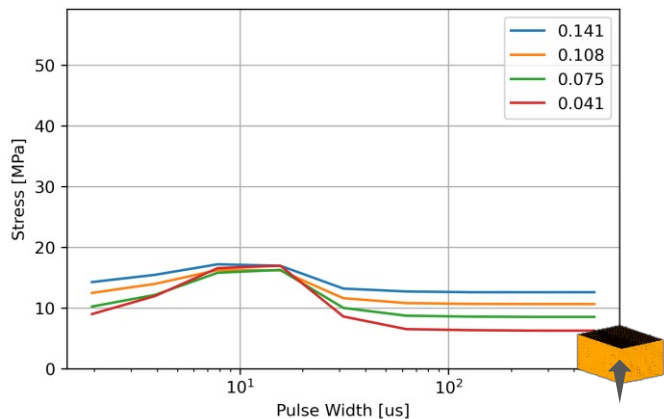


0.075"

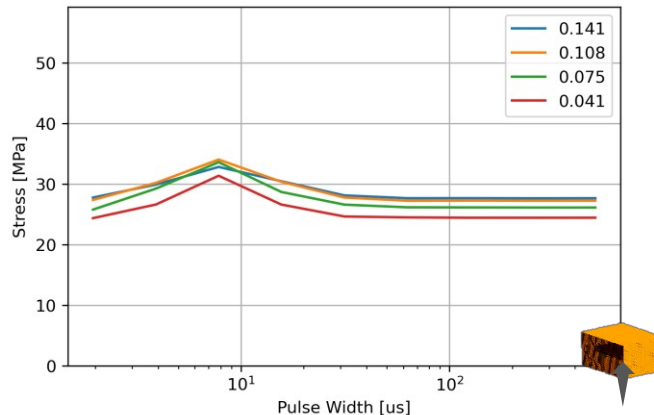


0.041"

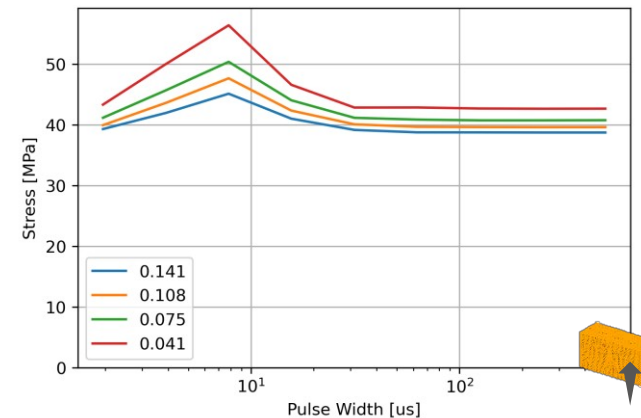
Peak Temporal, Spatial Average, Maximum Principal Stress



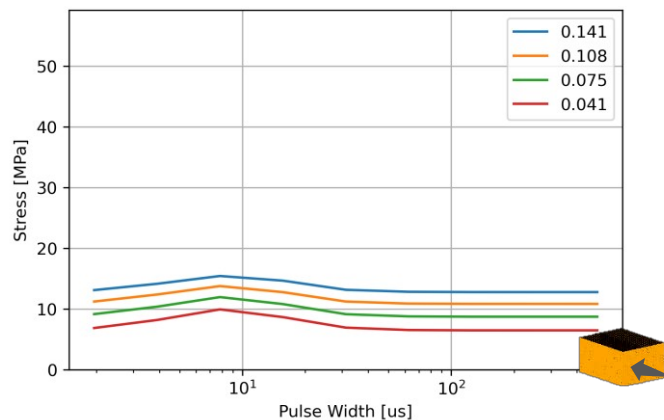
Peak Temporal, Spatial Average, Maximum Principal Stress



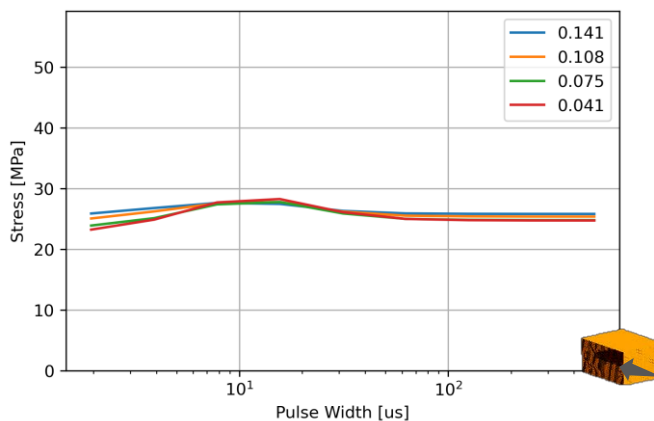
Peak Temporal, Spatial Average, Maximum Principal Stress



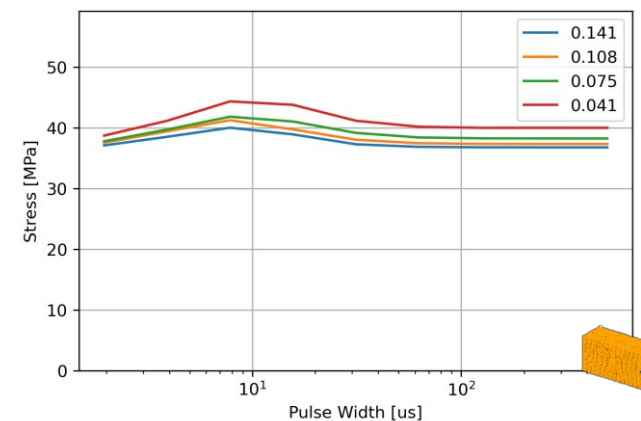
Peak Temporal, Spatial Average, Maximum Principal Stress



Peak Temporal, Spatial Average, Maximum Principal Stress



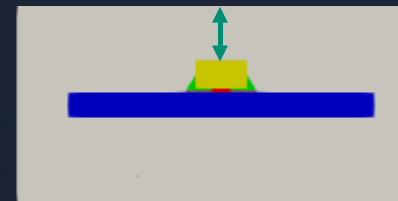
Peak Temporal, Spatial Average, Maximum Principal Stress



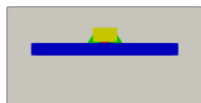
Proximity negligibly affects stress for Side Relief boundary condition.



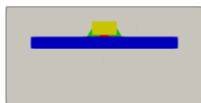
# Boundary Proximity: Maximum Capacitor Stress



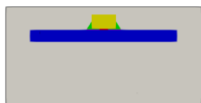
0.141''



0.108''

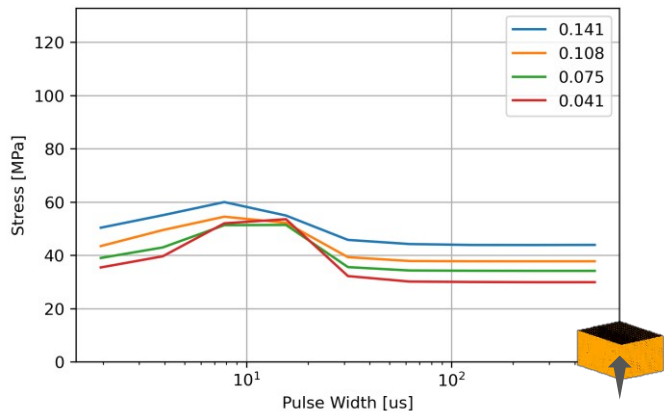


0.075''

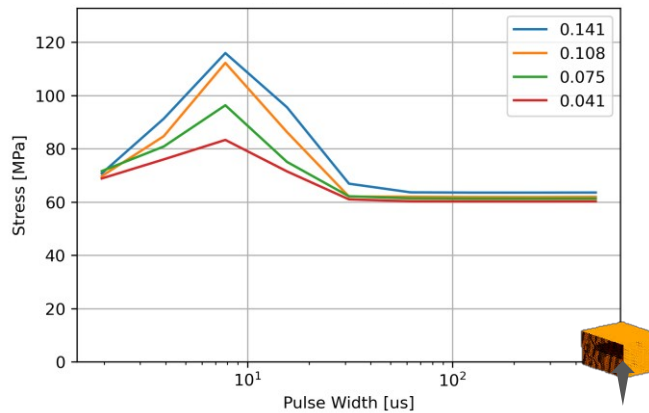


0.041''

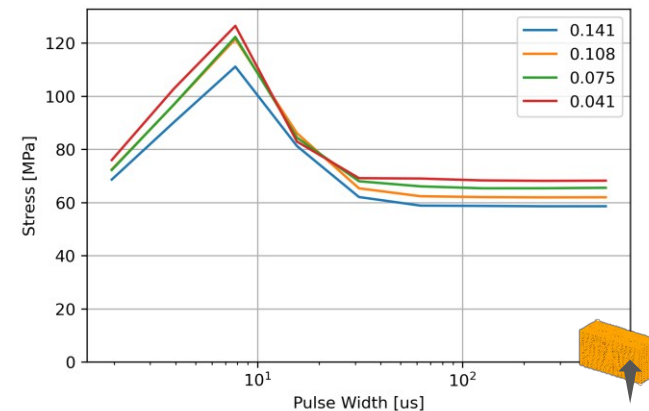
Peak Temporal, Spatial *Maximum*, Maximum Principal Stress



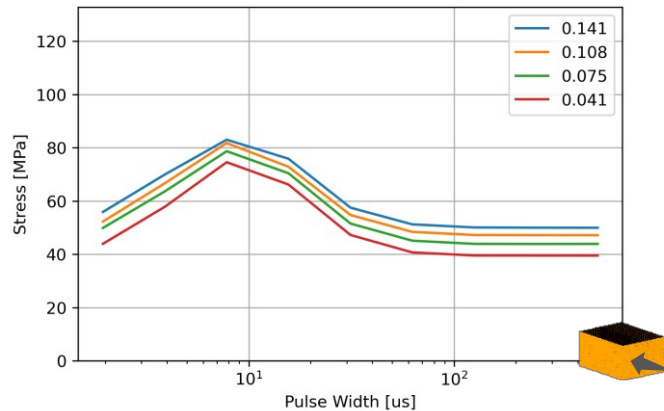
Peak Temporal, Spatial *Maximum*, Maximum Principal Stress



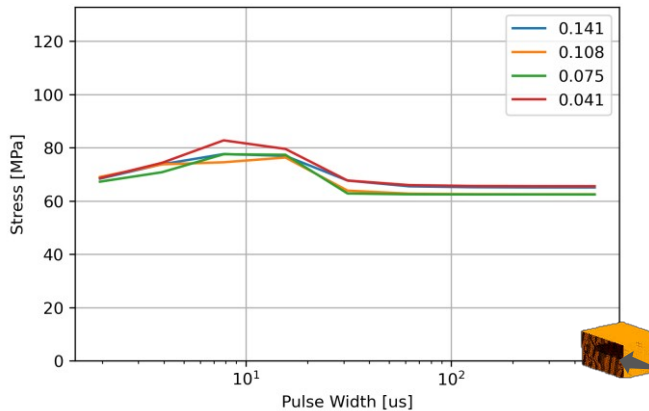
Peak Temporal, Spatial *Maximum*, Maximum Principal Stress



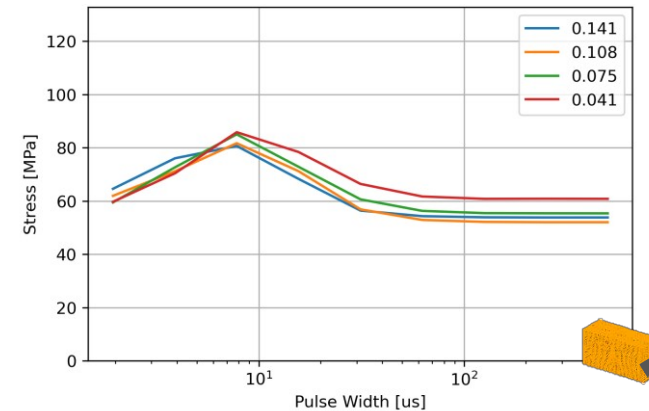
Peak Temporal, Spatial *Maximum*, Maximum Principal Stress



Peak Temporal, Spatial *Maximum*, Maximum Principal Stress



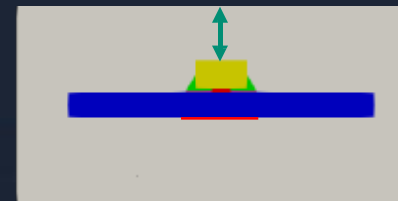
Peak Temporal, Spatial *Maximum*, Maximum Principal Stress



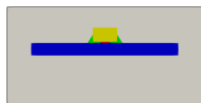
Relation of proximity to stress inverts in absence of reliefs.



# Boundary Proximity: Maximum PCB XX-Strain



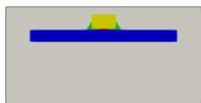
0.141"



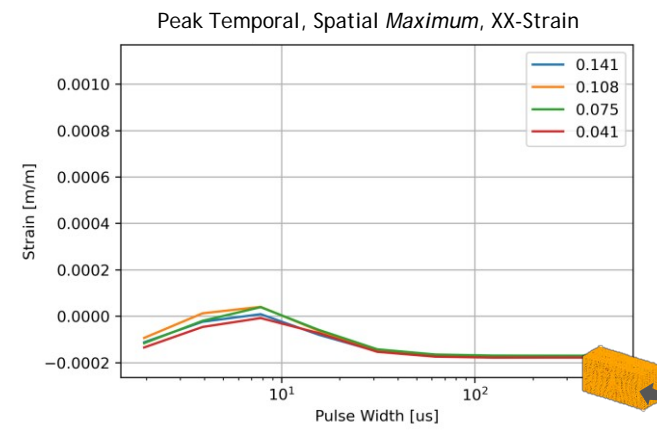
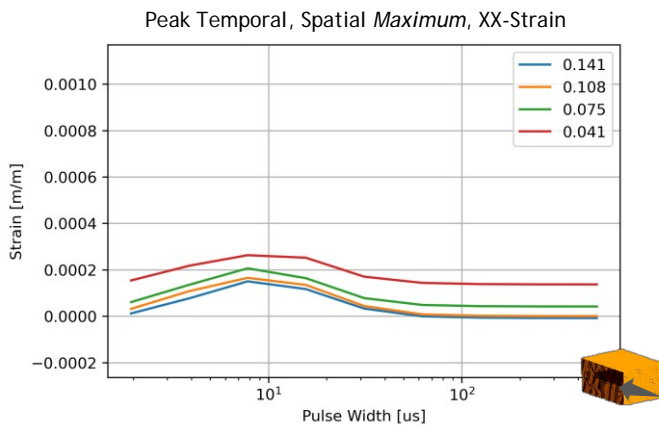
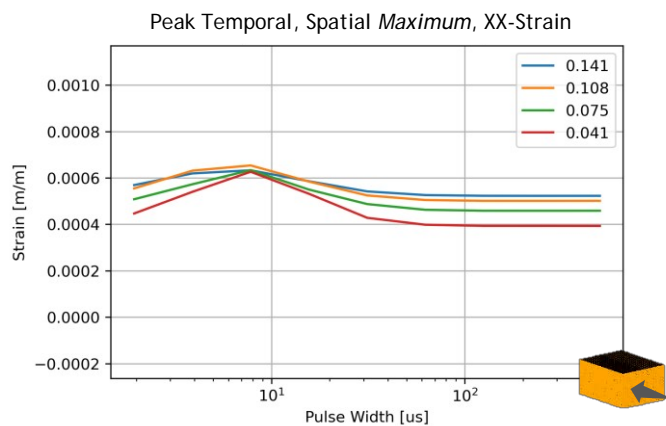
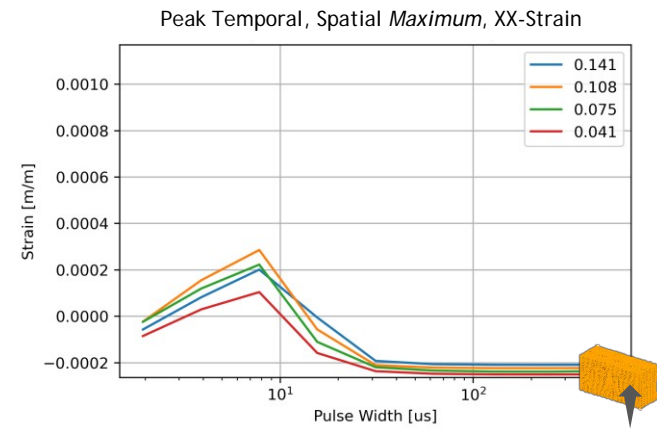
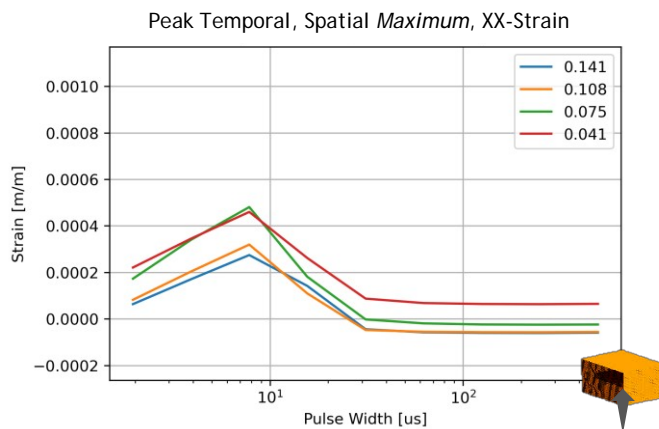
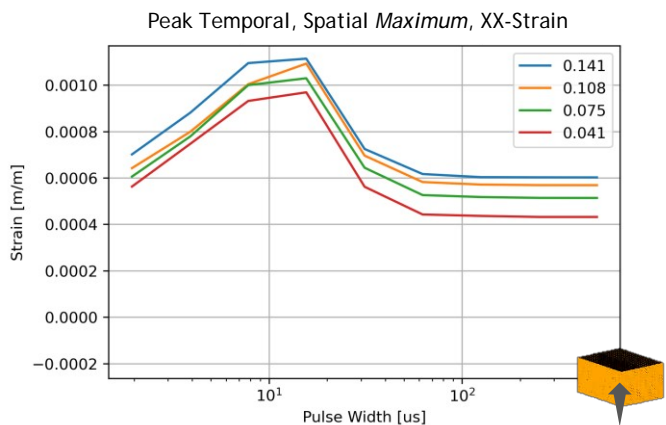
0.108"



0.075"



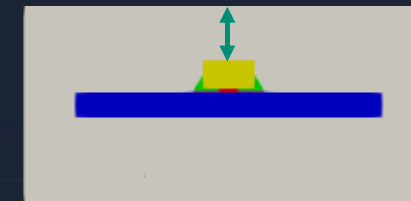
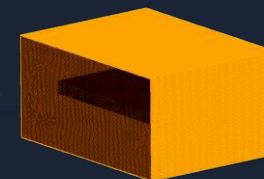
0.041"



PCB flexure behavior is complicated/dependent on variety of parameters.

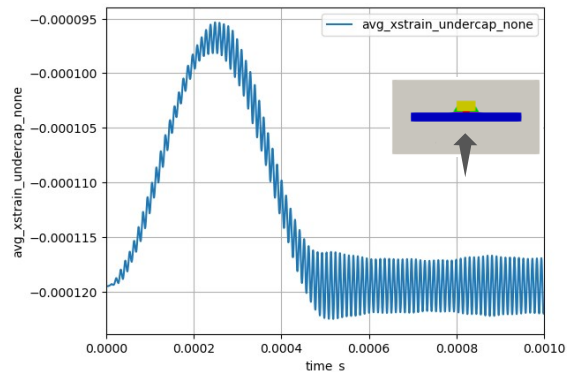


# Boundary Proximity: Nuances



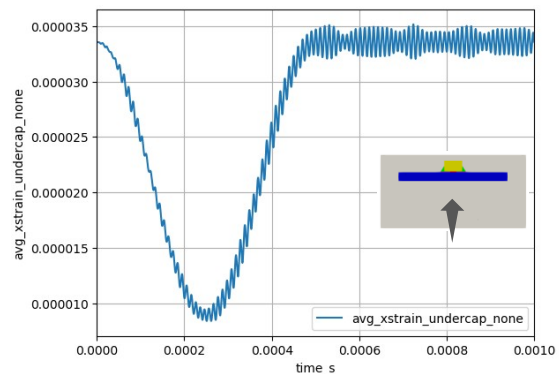
## Normal-to-PCB / Side Relief

PCB XX-Strain opposite capacitor



.141"

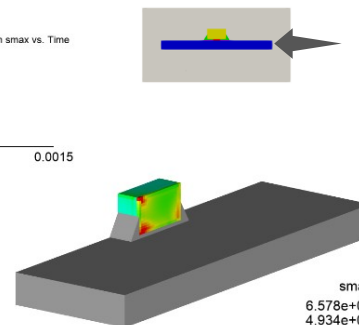
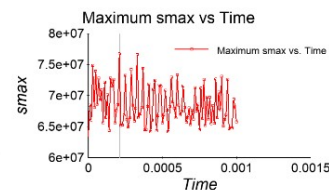
PCB XX-Strain opposite capacitor



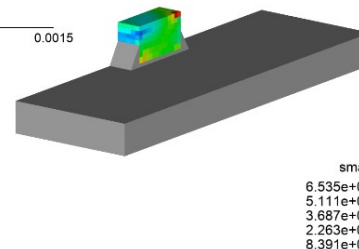
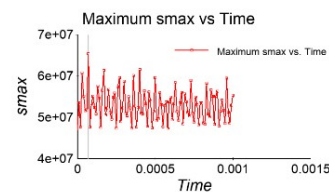
.041"

## Parallel-to-PCB / Side Relief

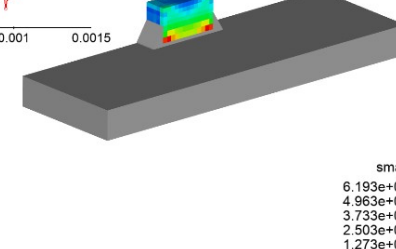
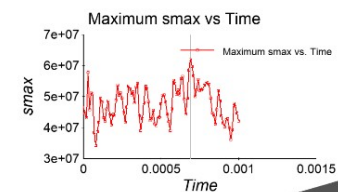
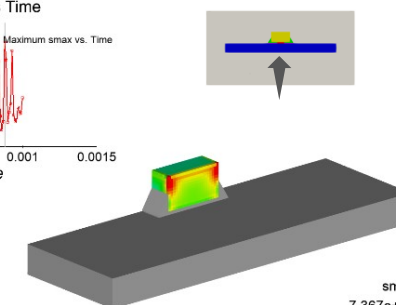
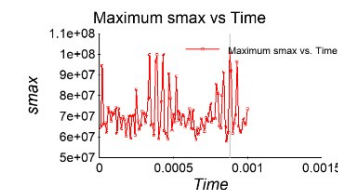
.141"



.041"





## Normal-to-PCB / Side Relief



Inconsistent, complex damage mechanisms confound intuition.

## Conclusions

- Strategic inclusion of relief mechanisms are critical for electronic survivability.
- The PCB *orientation* dictates fundamental displacement mode, the *relaxation condition* of the boundary in the direction of the displacement mode affects the resultant component stress state.
- Analyses of systems are vital, as complex, non-linear damage mechanisms can defy engineering intuition.
- Length of PCB has little effect in this study, longer PCBs could induce greater PCB deflection in other applications.
- Boundary proximity is directly related to the stress state in the absence of reliefs, but inversely related otherwise.
- Best performer<sup>1</sup>: Top Relief boundary condition & Normal-to-PCB loading direction. 
- 2<sup>nd</sup> performer<sup>2</sup>: Side Relief boundary condition & Parallel-to-PCB loading direction. 

<sup>1</sup>Does not account for components on opposite side of PCB.

<sup>2</sup>Possibly best case for real applications.





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