

[www.cadence.com](http://www.cadence.com)

[www.cadence.com/go/national-security](http://www.cadence.com/go/national-security)

Enabling the delivery and sustainment of secure and resilient capabilities to the warfighter and international partners quickly and cost-effectively

# **Better, Faster, Cheaper DoD Systems Through Commercial Electronics Design Best Practices**

*Leveraging the DoD Agile Electronic Hardware Emulation and Design Center and Tensilica To Realize The DoD AI Vision*

**J.S.B.Chew**     **Senior Global Group Director**  
**Chair, NDIA S&ET Division**

**23 Mar 21**

**cādence®**

# Who Is Cadence

**3,600+**  
R&D ENGINEERS

R&D INVESTMENT  
**\$936M**  
(~40% of revenue)

**1750+**  
FIELD ENGINEERING  
EXPERTS

PATENTS WORLDWIDE  
**1600+**

**US-based Company**  
**HQ, San Jose**  
**NASQ:CDNS**  
[www.cadence.com](http://www.cadence.com)  
[www.cadence.com/go/national-security](http://www.cadence.com/go/national-security)



**ONLY EDA Company Certified by DoD As A Trusted Supplier**  
<https://www.dmea.osd.mil/otherdocs/AccreditedSuppliers.pdf>

***Making the World a Better Place Through Intelligent System Design  
By Enabling First pass Success, Future Proofed Electronic Systems***

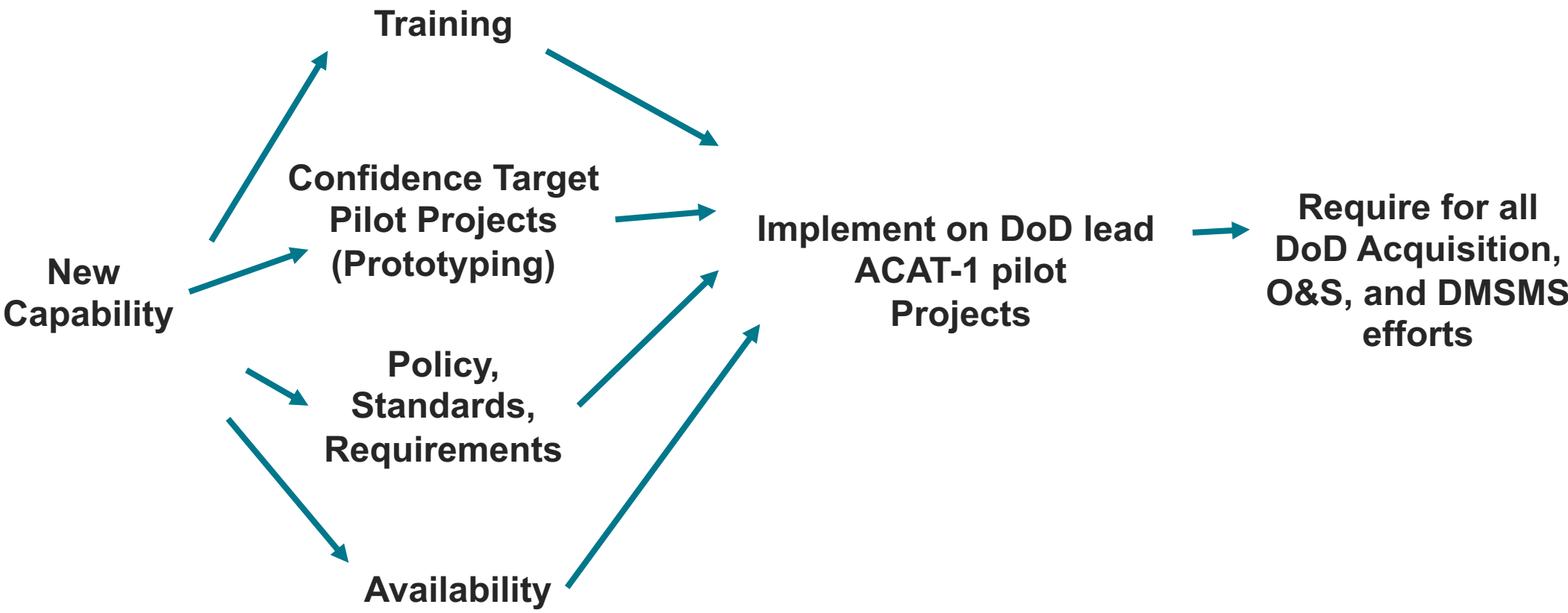


# Bottom Line Up Front

- **Cadence Design Systems (NASQ: CDNS) is an acknowledged leader in the Electronic Systems Design Enablement market**
  - Emulate Before You Fabricate
  - Intelligent Systems Design
  - We enable the Army's IVAS (*AI on the Edge*)
- **Since 2016, Cadence have been working to transition the Commercial Electronics Design Best practices to the DoD and Defense Industrial Base**
  - FY 17, FY 18 NDAA
  - National Defense Strategy
  - DoD funded pilot projects
- **DoD funded pilot projects has resulted in many “lessons learned”**
  - Identified deficiencies, challenges, and leverage points
  - Developed material to overcome and implement
- **If these “lessons learned” are leveraged, the DoD AI initiative can be accelerated and the quality of the finished product improved**
  - We want to help, in the appropriate fashion

***Cadence brings a unique and exclusive insight in to this challenge***

# Process To Implement New Capability to DoD Acquisition



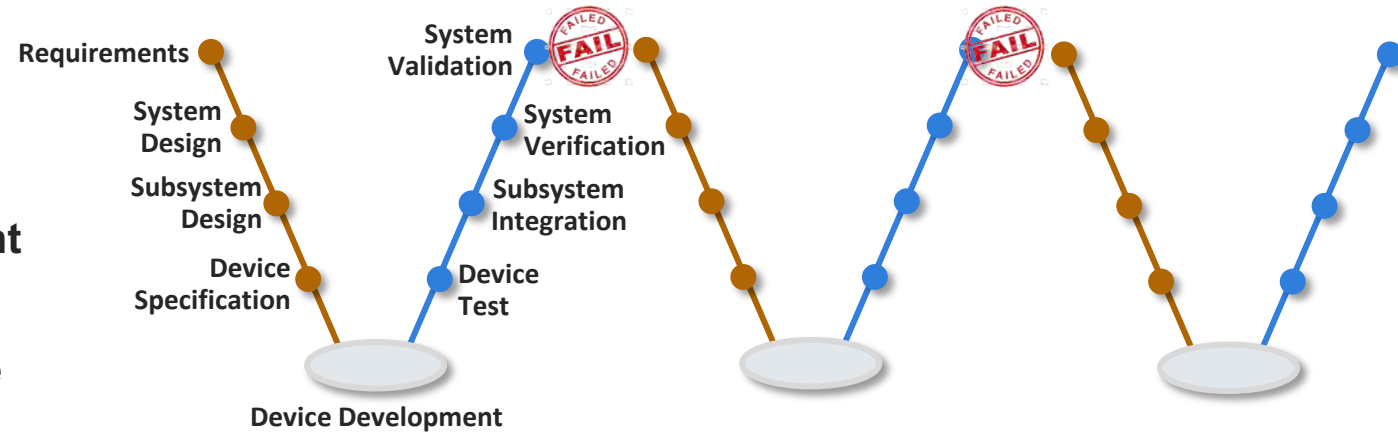
# ***Anecdotal Observations on US AI Activity***

- **Belief that AI/ML is a *Software Solution Only***
  - AI/ML systems are a combination of customized HW and SW systems depending on application
    - How many DevSecOp Guys Does it take to change a lightbulb?
    - They don't – that's a hardware problem
- ***Most US Electronic Manufacturers focus/core competency is in the communications aspect of the SOC/System; not in the AI/ML architectures***
  - Do not see an R&D Investment trend in AI for DoD
- **Lots of “R” funding, Not a lot of “D”**
- **Current *known* investment stems around Large/ Cloud based analytics/training applications**
  - Assuming huge platforms and data links
- ***Slim US focus on Edge based AI applications***
  - Will you have those data links during conflict?

# The DoD Acquisition/Development Culture

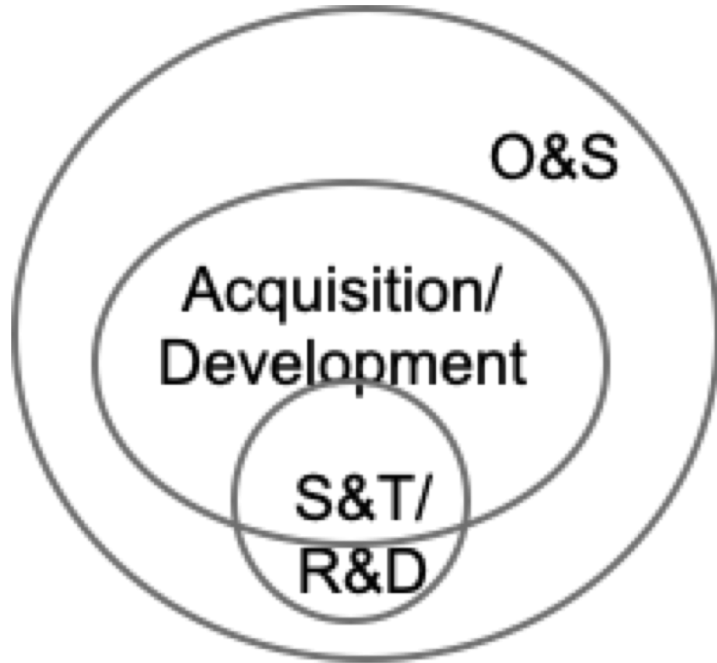
## Cost Plus Fixed Fee

- Build – Test – Rebuild - Test ...
- This process develops **HARDWARE** first , THEN **SOFTWARE** development starts
- Trainers developed after Prime Mission Equipment is built
- T&E performed **AFTER** Prototype Hardware/Prime Mission Equipment are Built
- Results in schedule slips and cost overruns
- Promotes performer culture of “Not Enough Time and Money To Do It Right, But Plenty Of Time and Money To Do It Over”



***Sustainment and Modernization NOT priority***

# ***The Commercial Electronic System Product Development Culture***



- **Funded Internally**
- **Can't Miss Christmas**
- **Emulate Before You Fabricate**
- **First Pass Success**
- **Sustainable and Modernizable at Launch**

***“People who are really serious about software should make their own hardware”***

***- Alan Kay***

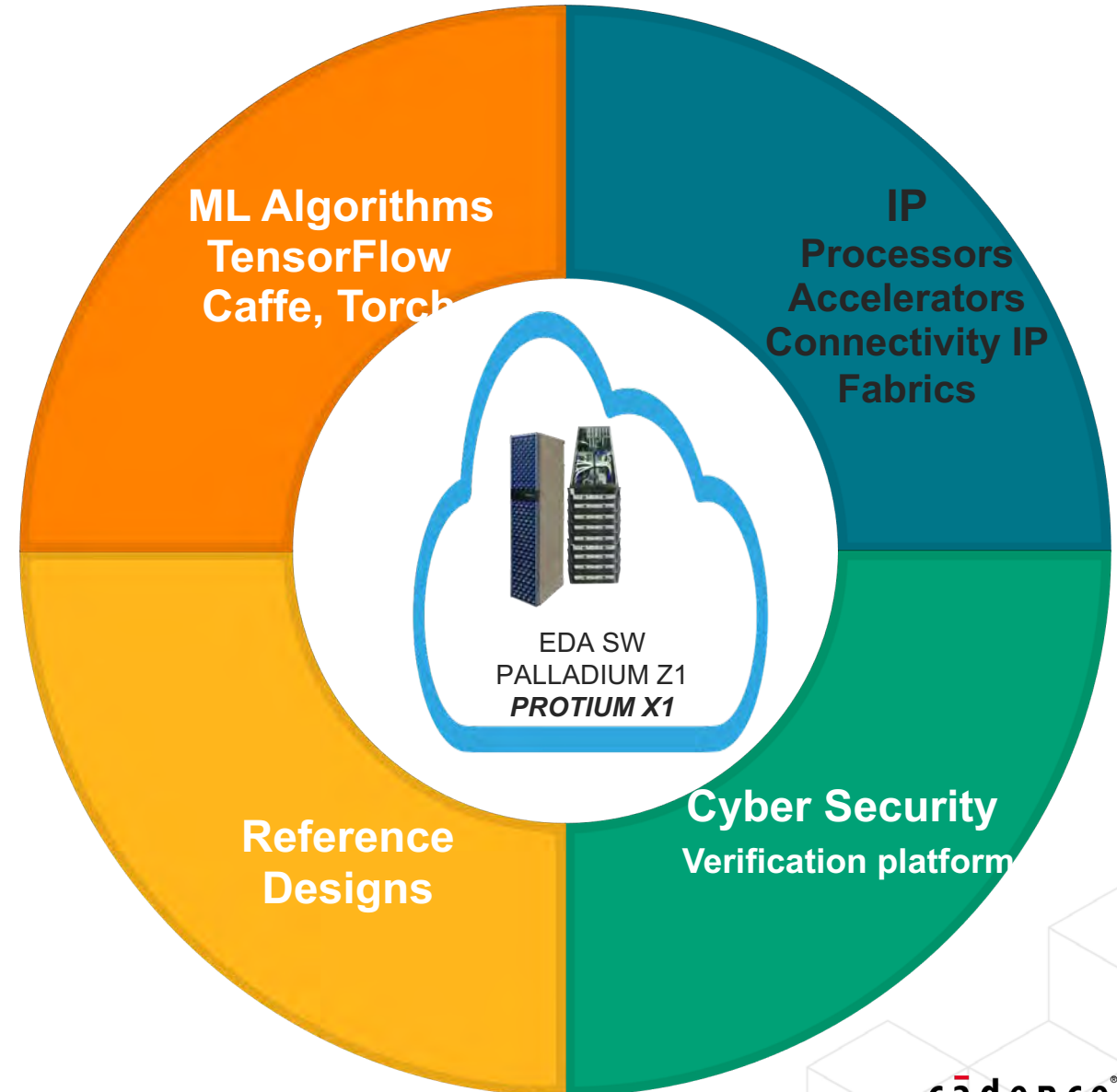
# ***How the Innovation Hub Can Advance the use of Edge Based AI To Ensure US Leadership***

- **Provide an environment for both research and DEVELOPMENT of AI electronic systems and which address the needs of those Applications**
  - University ( Research)
  - Start-ups ( Development)
  - Govt Primes ( Development)
- **Define key programs which can take advantage of AI Applications**
  - Target acquisition systems
  - Surveillance
  - Autonomous vehicles
- **Provide Initial Funding to Seed the Development**

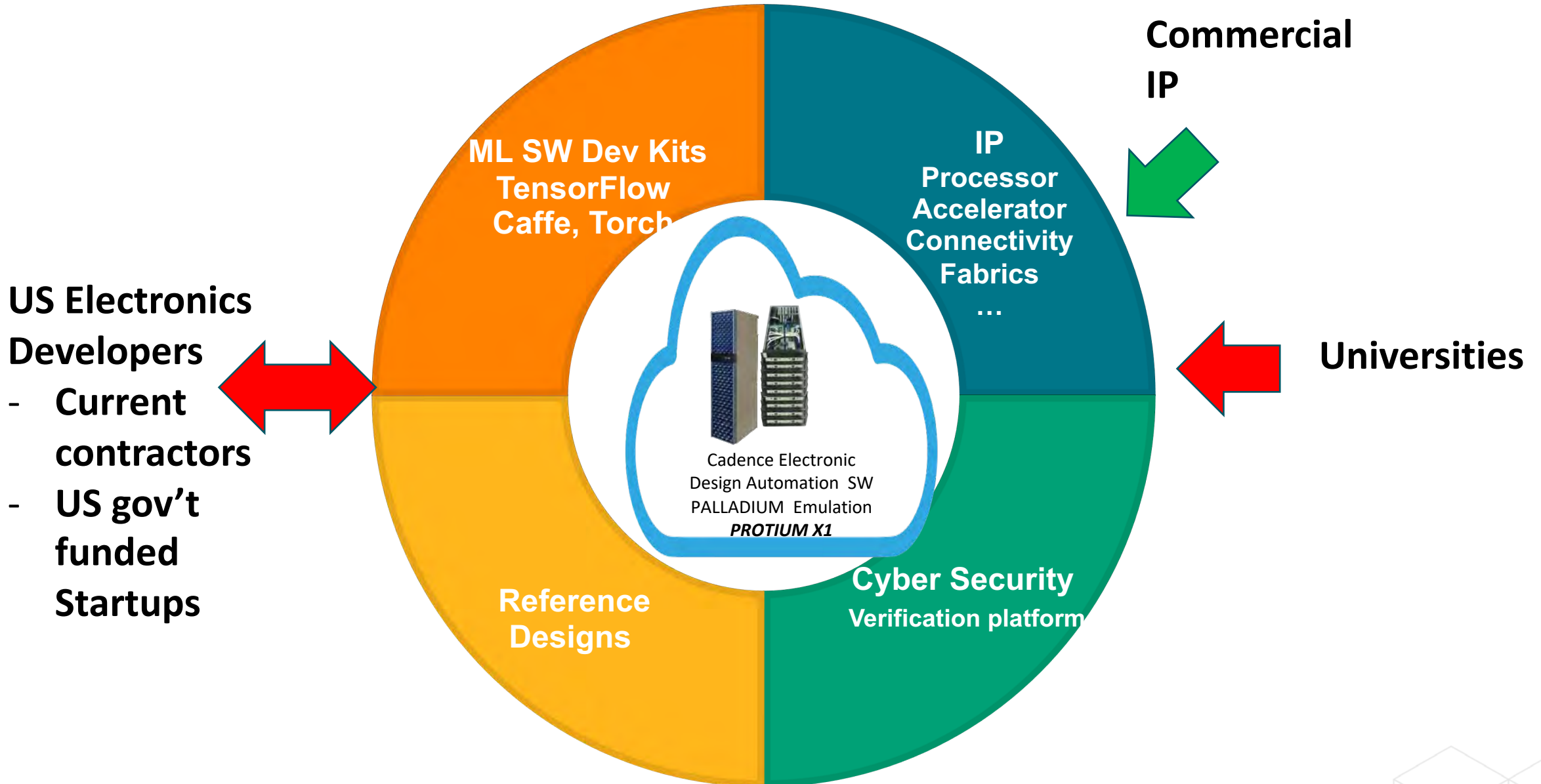


# AI Innovation Hub for US AI Edge System Development (HW/SW)

- **Cadence capabilities provide the Enabling technology blocks/methodologies for both Core and Edge Based Systems**
  - EDA SW-Develop/Verify hardware
  - IP/Reference designs
  - HW/ SW Development and Co-verification environment
    - VALIDATE SYSTEM (HW and SW) WORKS BEFORE YOU BUILD IT.
    - Emulation and Configurable Prototyping
  - Cyber Security Verification Platform
- **SW/Training algorithm development and test**



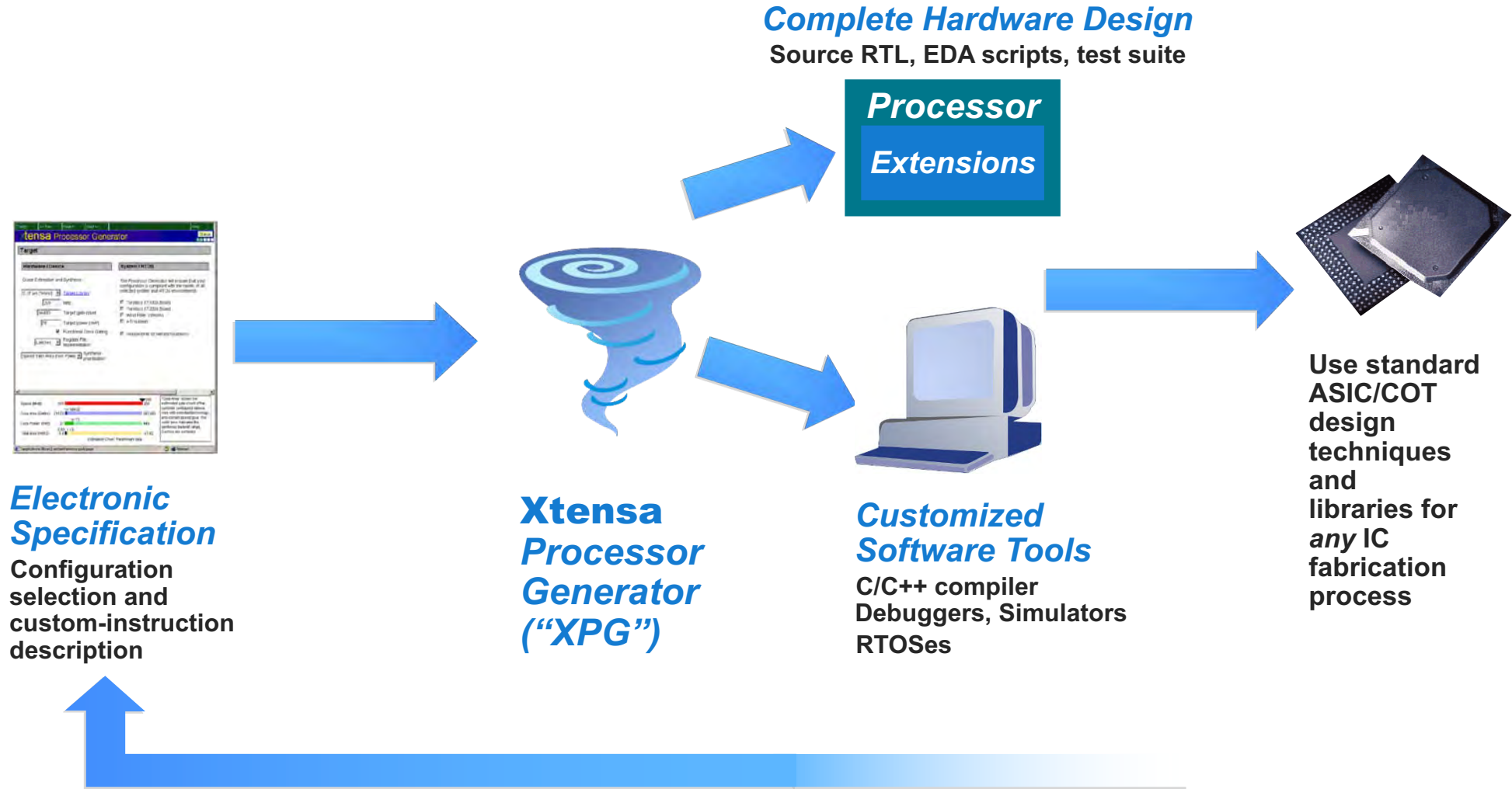
# NSCAI Innovation Hub for AI Cloud HW/SW R&D



# ***What is Tensilica: Benchmark Edge-based computing***

- **It is a RISC-based processor technology**
- **It is a Configurable and Extensible processor technology**
- **It is a design methodology**
- **It is an architecture design/analysis tool**
- **It is a set of software tools**
- **It is the “ARM of Audio”**
  - De facto standard for audio DSP

# How Does it Work?



# Tensilica® Products

## DNA

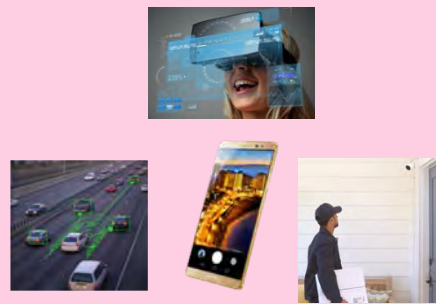
Standalone AI processor for AI at the Edge inference  
CNN, RNN, regression

### HiFi



- Audio pre- and post-processing
- Voice trigger
- Noise reduction, Audio encode and decode

### Vision



- Image and vision pre-/post-processing
- AI at the Edge
- SLAM, SGM

### Fusion



- Auto radar
- Consumer radar
- Always-alert sensor processing

### ConnX



- Narrow to wide band wireless
- LTE/LTE-A/5G
- Infrastructure and terminals

### Controllers/ Custom ISAs



- High performance DSPs, NPUs, CPUs
- Application specific data types
- Custom ISA, Special functions

Broad Range of Application Specific DSPs

Custom

Automated User-Defined Customization (TIE)

Xtensa® Processor

# DoD Federated Emulation and Design Center (WPAFB, OH)

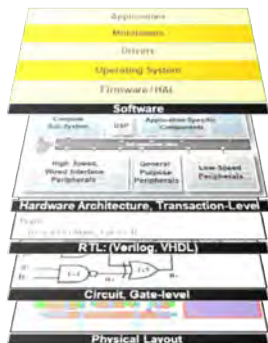
Located At Wright-Patterson AFB



Systems



Board & Package

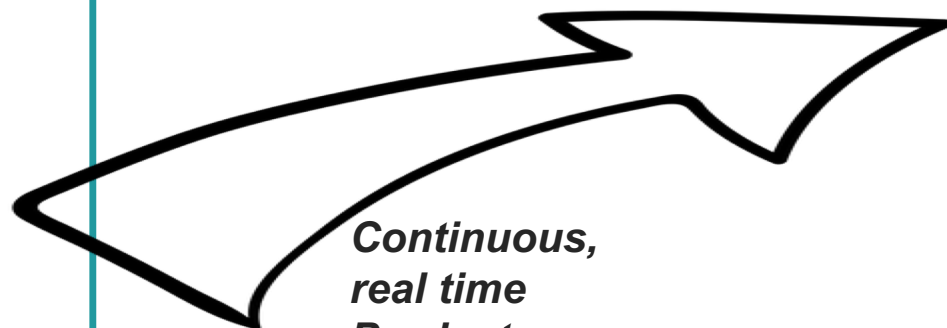


Hardware/Software Co-Design



IP & Subsystems

## Emulate Before You Fabricate



Continuous, real time Product development management

- Hardware Development
- Systems Integration
- System/subsystem, Performance Analysis
- Thermal, EMI, Power systems analysis

**Palladium Emulation**

Hardware

Software

Compile

- Software development
- *Digital Twin* for DevSecOps Development
- *Digital Twin* for system, subsystem developers
- *Digital Twin* for trainers, operators, maintainers

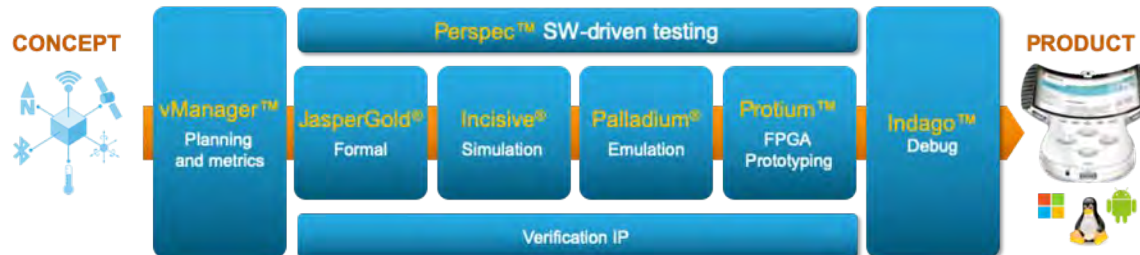
Digital Twin

DUT

Same Physical Interfaces

**Protium Prototyping**

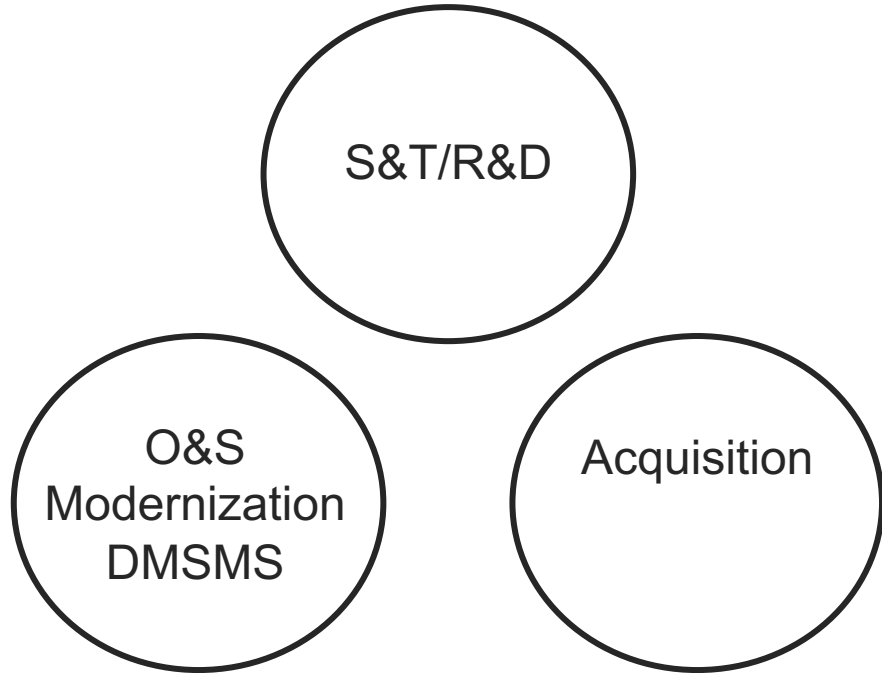
All Groups working on Common design, via Cloud, resulting in Trainers Developed and In Use Well Before Capability Is Fielded



# Impact/Payoff To DoD

## Continuous, Agile Improvement; No More Block Upgrades

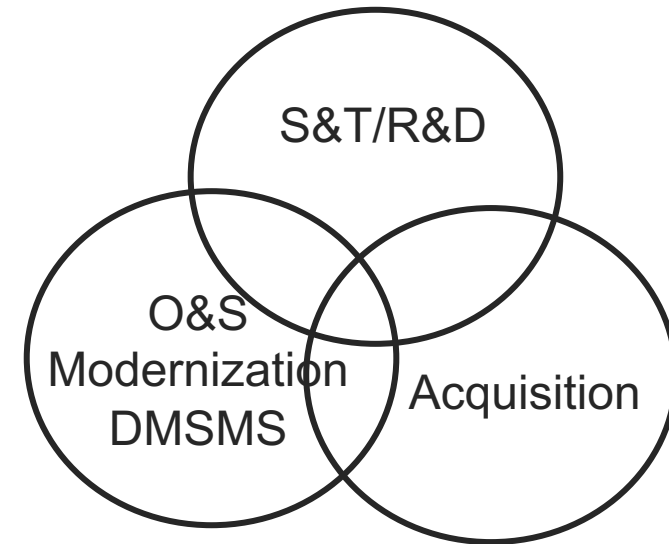
### Current



**Three separate activities**

***(Illustration Idea by CDR Jon Connelly)***

### Future



**Continuous Improvement**

**All Groups working on  
Common design, via Cloud, resulting in  
Rapid Agile Fielding of New Capabilities  
on an "As Needed" Basis**

cā dence®

© 2019 Cadence Design Systems, Inc. All rights reserved worldwide. Cadence, the Cadence logo, and the other Cadence marks found at [www.cadence.com/go/trademarks](http://www.cadence.com/go/trademarks) are trademarks or registered trademarks of Cadence Design Systems, Inc. Accellera and SystemC are trademarks of Accellera Systems Initiative Inc. All Arm products are registered trademarks or trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. All MIPI specifications are registered trademarks or service marks owned by MIPI Alliance. All PCI-SIG specifications are registered trademarks or trademarks of PCI-SIG. All other trademarks are the property of their respective owners.

