DoD Microelectronics Overview - on behalf of Honorable Heidi Shyu

NDIA Electronics Division Summer Meeting

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OUSD (R&E) - Critical Technologies

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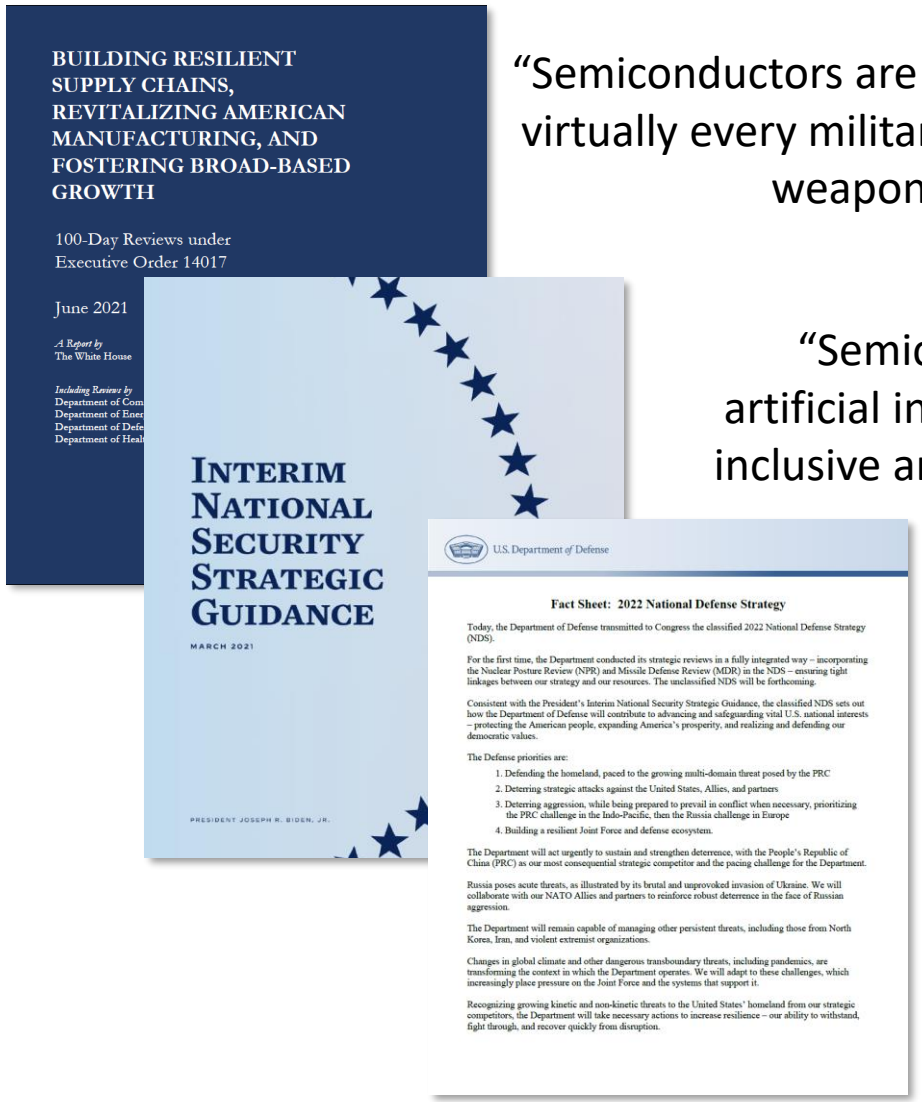
Microelectronics a “must-win” technology for DoD



“Semiconductors are essential to national security. . . . They are fundamental to the operation of virtually every military system, including communications and navigations systems and complex weapons systems such as those found in the F-35 Joint Strike Fighter.”

“Semiconductors are key to the “must-win” technologies of the future, including artificial intelligence and 5G, which will be essential to achieving the goal of a “dynamic, inclusive and innovative national economy” identified as a critical American advantage in the March 2021 Interim National Security Strategic Guidance.

“Building enduring advantages . . . getting the technology we need more quickly, and making investments in the extraordinary people of the Department, who remain our most valuable resource.”

DoD Microelectronics Vision

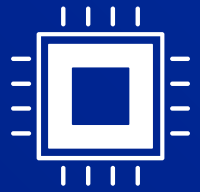
Vision Statement:

Guaranteed, long-term Access to Measurably Secure Microelectronics

enabling Overmatch Performance

and increasing Military Operational Availability and Warfighter Combat Readiness

Ensure timely access to measurably secure and affordable ME technology



Motivate programs and their primes to modernize and exploit the most capable ME

Leverage tools, policies and enforcement to reduce or eliminate costly sustainment issues

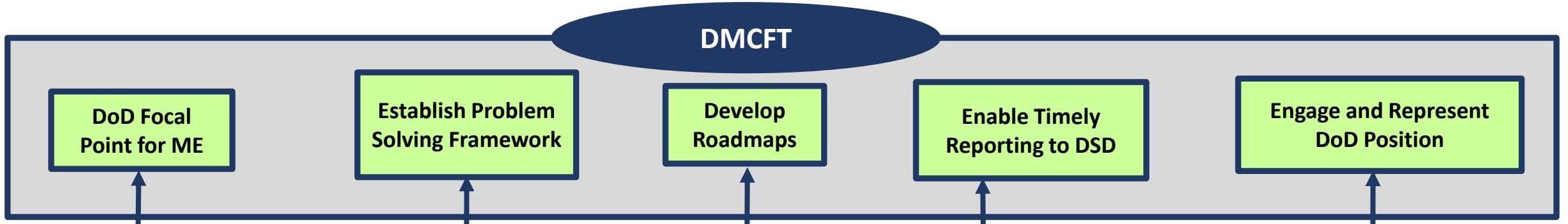
Centralize knowledge in a DoD "front door" organization to augment decentralized execution

Increase ME discovery and innovation, and accelerate transition into DoD systems

Contribute to and influence interagency and national efforts to grow ME capabilities to meet national security needs

Cultivate a right-sized workforce with the right skills at the right place and the right time

Defense Microelectronics Cross Functional Team (DMCFT) Objectives



To provide a focal point addressing the DoD's highest priority Microelectronics challenges.

To develop roadmaps that define the optimal course of action with specific results-oriented objectives.

To actively engage and represent the DoD's position in interagency coordination, coordination with Congress, and coordination with the Executive Office of the President

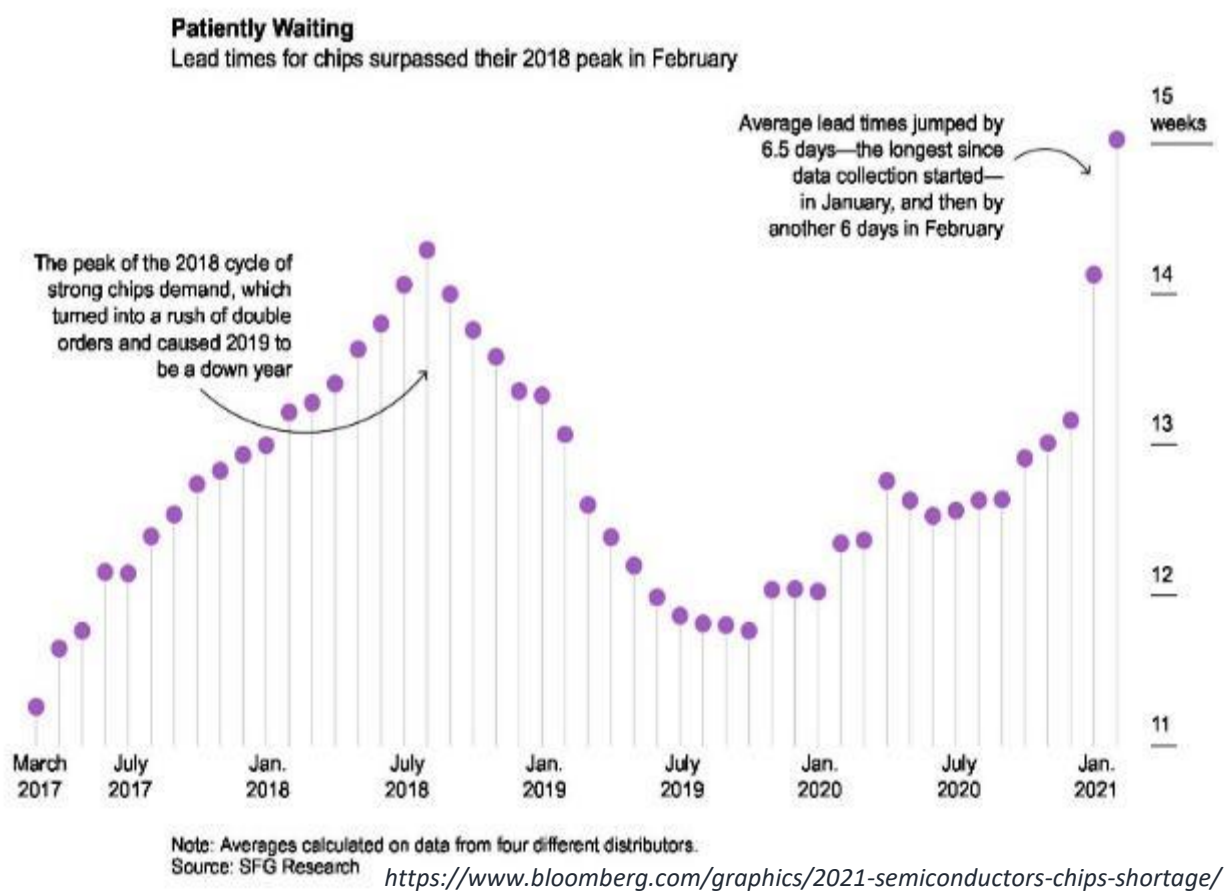
To establish a problem solving framework with sufficient representation from the Office of the Under Secretary of Defense for Research and Engineering (OUSD(R&E)) and the OUSD for Acquisition and Sustainment (OUSD((A&S)), the Military Departments, and other DoD Components to identify and recommend solutions concerning defense microelectronics.

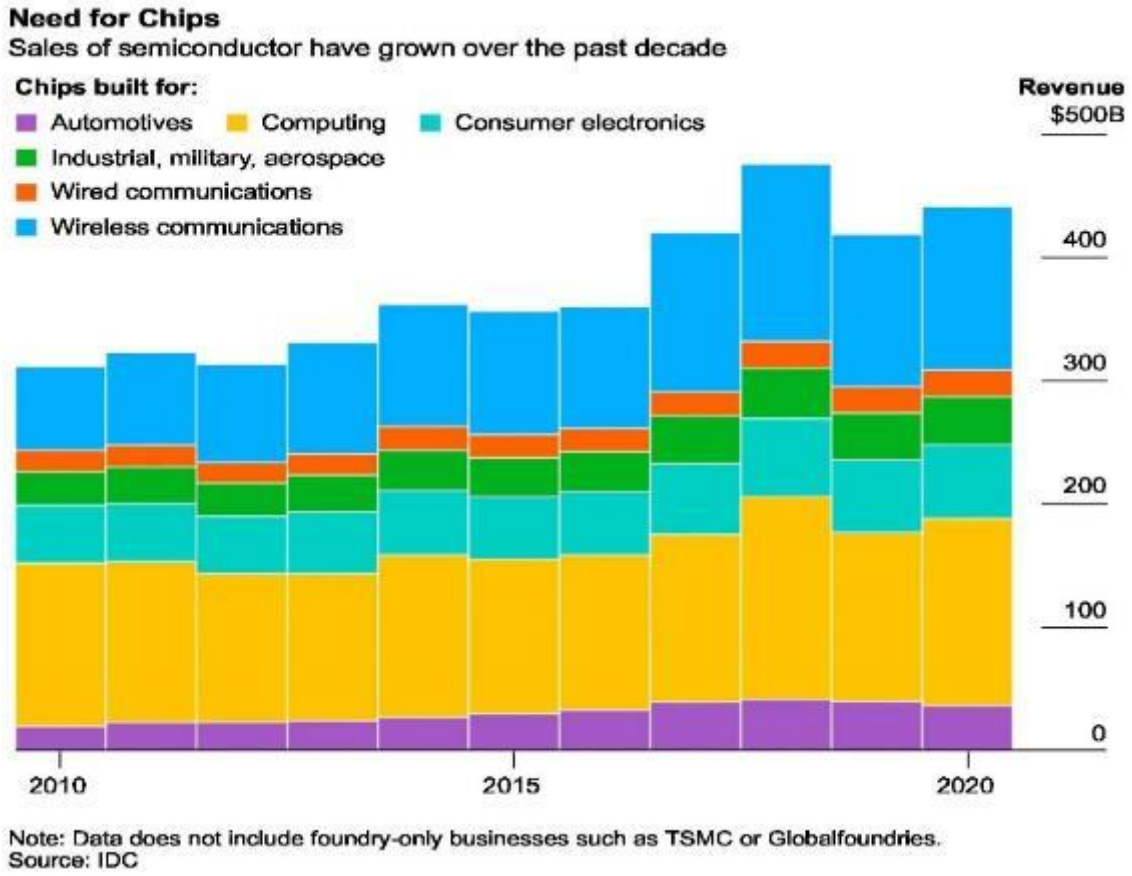
To enable timely communication and reporting to the Deputy Secretary of Defense (DSD) that ensures top-level decisions are made internally before being communicated outside the Pentagon.

Establish a comprehensive defense microelectronics strategy to include:

- *Holistic DoD approach that strengthens the domestic microelectronics industrial base*
- *Detailed plan to develop and transition microelectronics technology into DoD systems.*

Impact of COVID on Global Supply



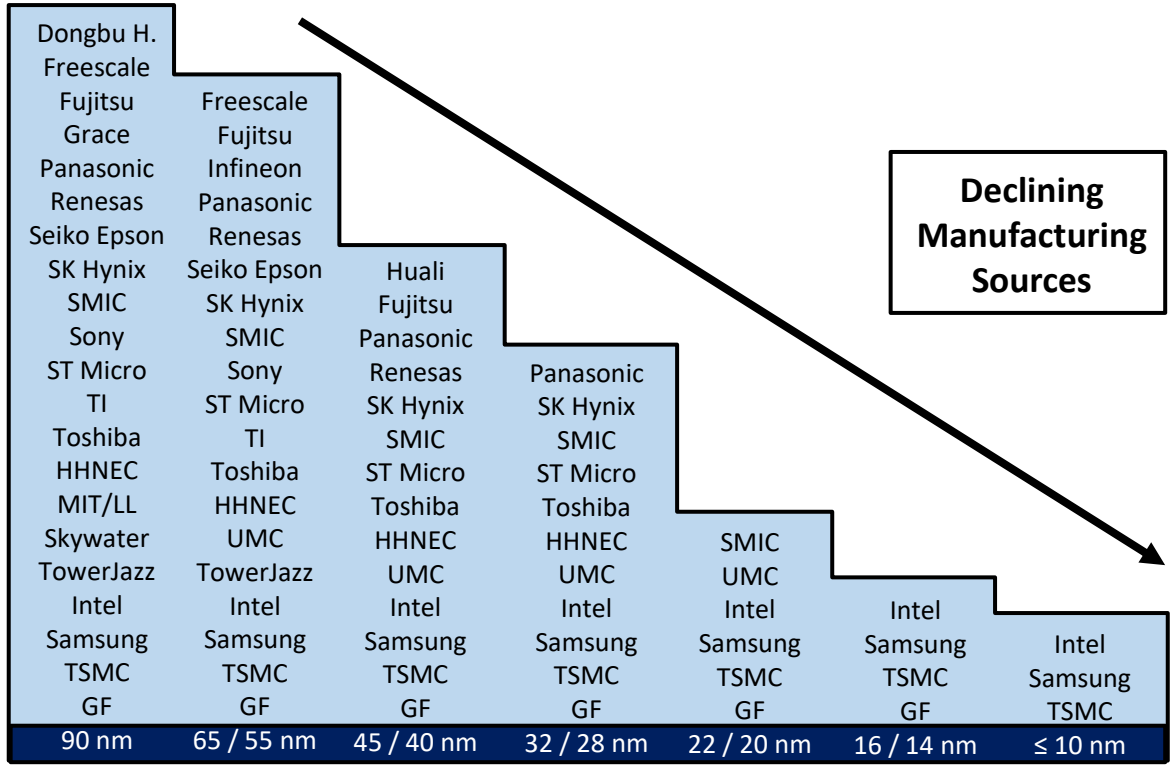


https://www.bloomberg.com/graphics/2021-semiconductors-chips-shortage/

- In February [2021], lead times—the duration between when an order for a chip is placed and when it actually gets filled—stretched to 15 weeks on average for the first time since data collection started in 2017
- The crunch has sideswiped the General Motors, and Volkswagens of the world and swung politicians from Washington to Beijing into crisis control

DoD Faces Foundry Consolidation Challenges

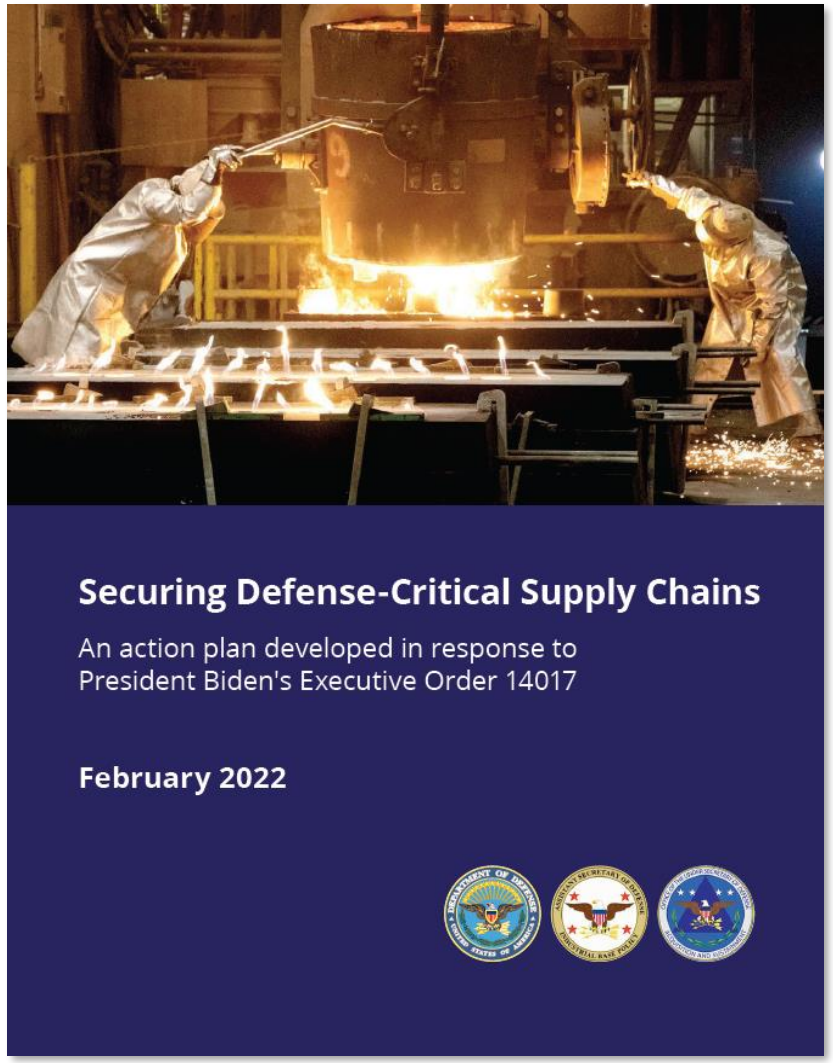
90-nm Fully depleted silicon on insulator (FDSOI) @ SkyWater Initial access rolled out in 2021



Derived from a chart originally from the General Services Administration (GSA)

DoD requires a multi-vendor, assured, pipeline of critical microelectronics across several generations of technologies in a diminishing global supply chain

Microelectronics Supply Chain Visibility



"Supply Chain Visibility: DoD is still building visibility into the sub-tiers of the microelectronics supply chain; until there is greater visibility, it will be difficult to identify certain supply chain threats, vulnerabilities, and risks. Visibility is further eroded by system-level (next-level assembly comprised of multiple microelectronics components) manufacturers who simply seek the lowest cost producers and are source agnostic."

https://media.defense.gov/2022/Feb/24/2002944158/-1/-1/1/DOD-EO-14017-REPORT-SECURING-DEFENSE-CRITICAL-SUPPLY-CHAINS.PDF

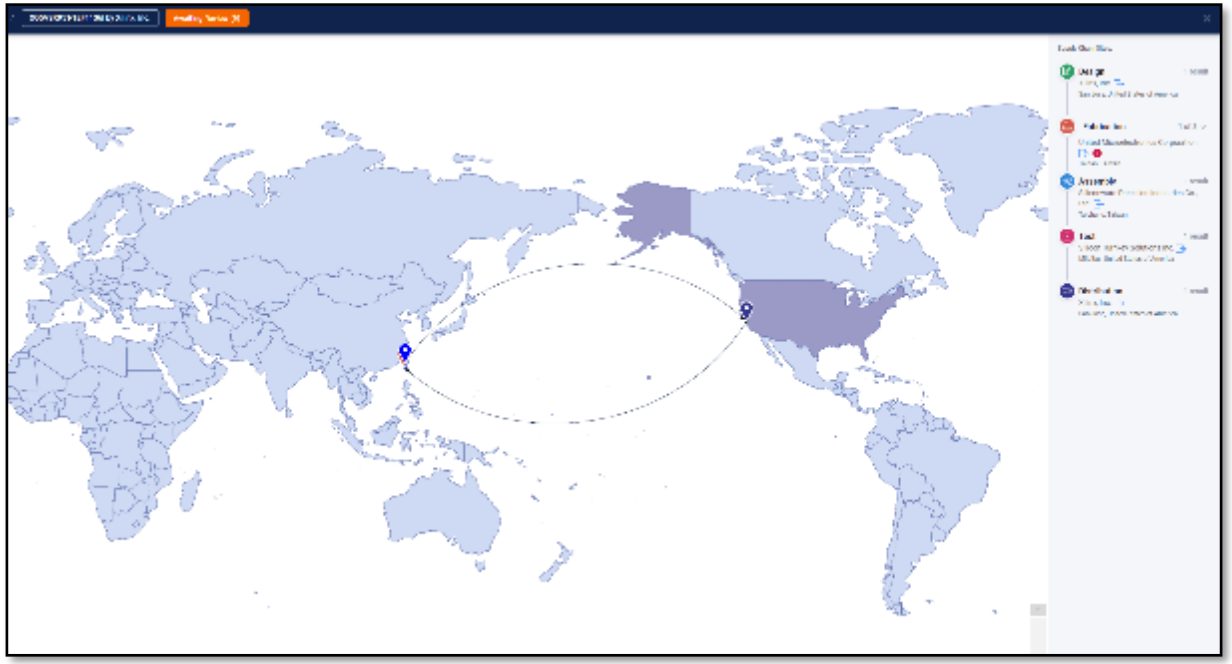
Automated Microelectronics Analysis and Reporting Optimization (AMARO)

Supply Chain Challenges

- **Existing tools unable to provide aggregate threat and vulnerability data on a collection of microelectronics parts (BOMs)**
- **Existing tools unable to determine which third-party sites specific semiconductor devices move through**

AMARO Tool

- **Can map microelectronics lifecycle across the entirety of its supply chain, and identify possible threats and vulnerabilities**
    - Can assess across a Bill of Materials (BOM)
- **Tool designed to address needs of DoD Programs, JFAC, CI Community, and Senior Decision Makers**
- **Can aid in high-level, strategic questions**
    - "Impact to DoD if Country X invades Country Y?"
    - Natural disaster "what-if" scenarios
    - Support to CFIUS cases



Market for Secure Microelectronics: National & Economic Infrastructure

AI & Supercomputers
DOE, NASA

Energy Infrastructure National Grid
DOE, NRC

Banking, Medical and Other Sensitive Verticals
DHHS, FDIC, OSHRC

Next-Gen Comms
DHS

Cyber Security
DHS

Transportation
DOT, NTSB, FAA

Dept. & Agency Data Centers
ODNI

Weapons Systems
DOD ≈1% of demand

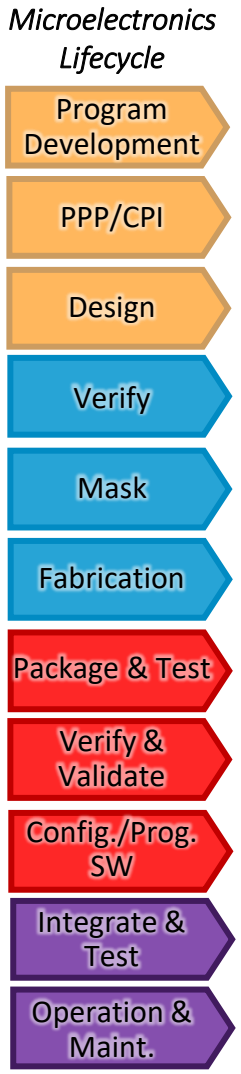
Aggregated Market is ≈24% of U.S. Demand

Access to Measurably Secure ME will serve this critical infrastructure market

- Domestically designed, manufactured, packaged and tested parts that meet U.S. security and safety standards
- Ensure access to a forecasted aggregated demand of SOTP and Legacy Technologies (designs remain robust over a 10+ year PoP)

A "whole of nation" approach to access Measurably Secure ME

Implementing Proven and Evolving Approaches to Address Threats and Vulnerabilities in the Microelectronics Lifecycle



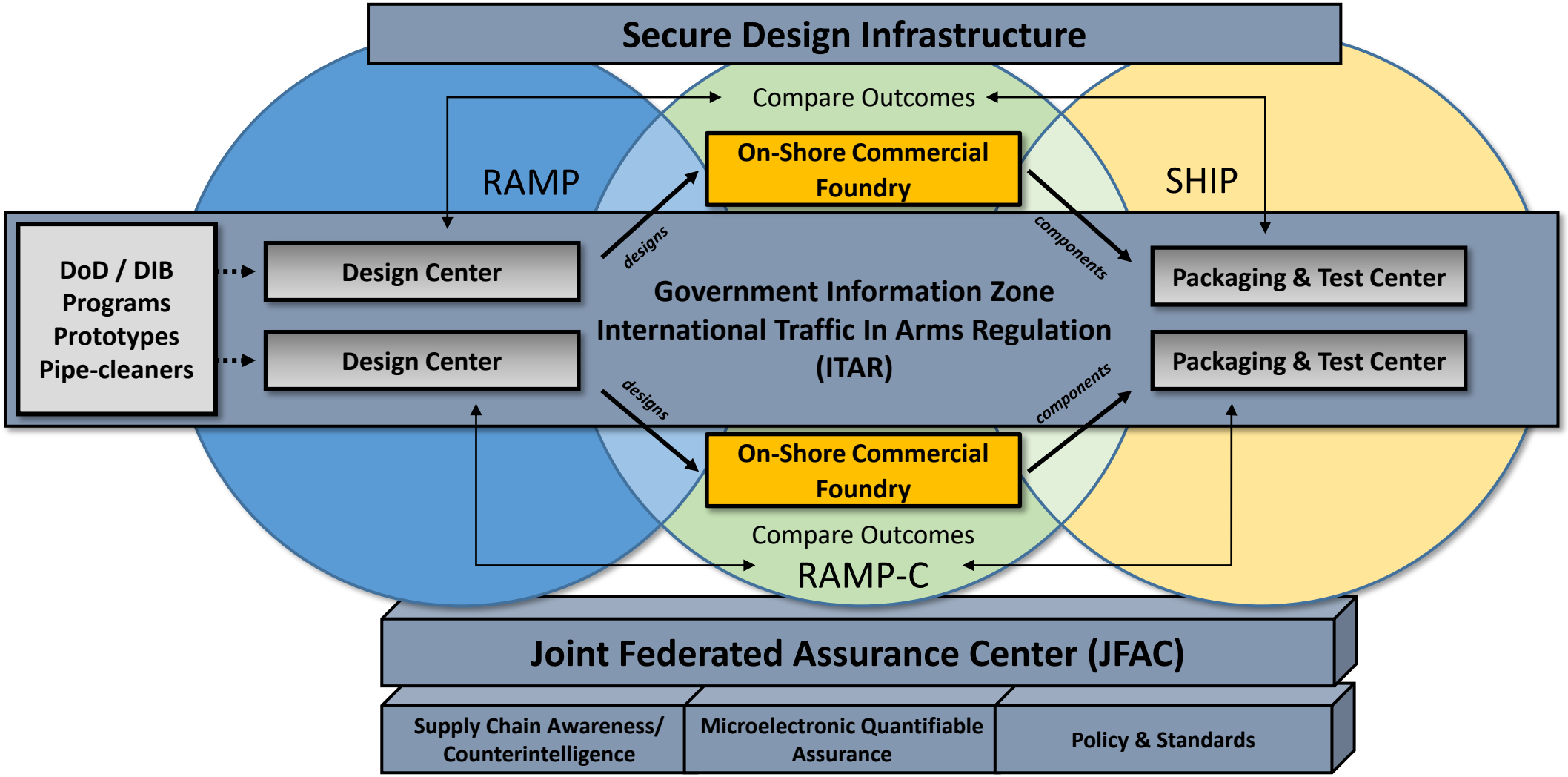
DoD Microelectronics Assurance Framework (MAF)

- Approach under development utilizes risk-based decision making to ensure systems can manage evolving and insider threats present in today's global microelectronics ecosystem

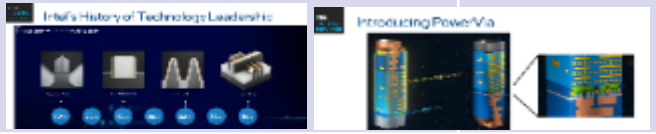
"Trusted Supplier" Approach

- Continues to secure critical technologies through accreditation based on commercial standards

T&AM Program Enabling Access to State of the Art (SOTA)



Access to State of the Art (SOTA) Roadmap

Fiscal Years →	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032+
Foundry Access		**Access to SOTA US commercial foundries for DoD specific designs**									
		Establish 2 runs per year in commercial ≤ 22nm node technology for DoD Specific Designs					*U.S.-located, leading-edge wafer fabrication capacity of 25K wspm & qualified COTS products & volume*				
RAMP		**Rapid Assured Microelectronics Prototypes**									
			Demonstration of Secure Design Capability via 3 Prototype physical design by the DIB in SOTA (defined as ≤ 22nm node Si CMOS) technology nodes.				*Cloud based commercially scalable, quantifiably assured, design and manufacturing flow capability*				
RAMP-C		**RAMP-Commercial**									
		Test Chip Design, Yield 5k/wafer starts 3 COTS product designs verified		*Low Volume quantifiably assured (QA) production*			*High Volume (25k/wpms) leading edge (<7nm) foundry capability for QA dual-use COTS & custom DoD ICs*				
Cloud and EDA		**Emulation Pathfinder for QA Design Flow**									
			JSF F35 & PEO SUB prototype demonstrations of emulation based QA design flows				*Qualified emulation based QA design flow capability*				
SAHARA		**Structured Array Hardware for Automatically Realized Applications.**									
		FPGA Conversion and Secure Design Demonstrated	*Prototype chip Demonstrated (50M gates)*				*Fully developed SAHARA capability to efficiently convert existing FPGA designs to Structured ASIC, at an onshore SOTA foundry with security*				

LEGEND

Enhanced Capabilities

Key Milestones *Unfunded Option*

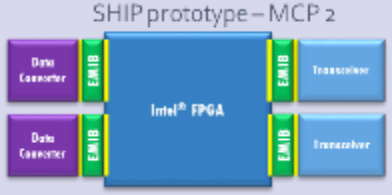
Major Investments to Mature the Domestic SOTA Microelectronics Ecosystem

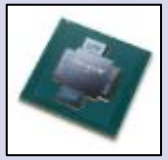
Future SOTA Microelectronics Needs

- Domestic access to mature SOTA materials, foundries, and packaging
- Ecosystem alignment to DIB and POR

Access to Advanced Packaging Roadmap

Fiscal Years →	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032+
State-of-the-art (SOTA) Heterogeneous Integrated Packaging (SHIP) - Digital	**Digital Packaging and Test Capability**				**Digital Packaging Access Model Implementations**						
				Sustainable Access Model in Place				*Sustainable Access Model Stand Ups*			
					Advanced Digital Packaging Capability Development						
				Prototype Demonstrator Multi-Chip Packages				*Packaging Capability Development Projects*			
					Advanced Digital Packaging Technology Maturation						
			Demonstrator Chiplet				*Technology Maturation & Prototyping Projects*				
State-of-the-art (SOTA) Heterogeneous Integrated Packaging (SHIP) - RF	**RF Packaging and Test Capability**				**RF Packaging Access Model Implementations**						
							Sustainable Access Model Stand Ups				
				Packaging Technology Releases	*Factory Setup Complete*		**Advanced RF Packaging Capability Development**				
			Assembly Design Kits					*Packaging Capability Development Projects*			
							Advanced RF Packaging Technology Maturation				
				Prototype Demonstrator Multi-Chip Packages					*Technology Maturation & Prototyping Projects*		
Specialty Capability	**Secure Packaging and Test Capability**				**Additional Secure Packaging & Test Facilities**						
									Secure Packaging & Test Stand Ups		
				Prototype Delivery	**DoD Unique Packaging Capability Development**						
											Packaging Capability Development Projects





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Enhanced Capabilities

Key Milestones

Sustained access to domestic SOTA advanced packaging for DoD system modernization

Future Advanced Packaging Needs

- A self-sustaining model for DoD and the DIB to procure cutting edge microelectronics in a high mix – low volume environment.

Radiation Hardened Microelectronics (RHM) Roadmap

Fiscal Years →	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032+
RH by Process	HNY Legacy 150-nm SRH, Title III SkyWater 90-nm FDSOI w/ Cu BEOL) *Demonstrate design and process capability with radiation tested chip, TRL-6*				*Fully qualified 2nd US source of Strategic RHM (SRHM) enabling new mission functionality with 2-3x capability improvement, TRL-8*						
RH by Design	GF Legacy 45-nm, Title III GF 12-nm & Intel 16-nm *Demonstrate design and process capability with radiation test chip, TRL-6*			*Two new sources of SRHM enabling onboard processing capability with 100x capability improvement, TRL-8*	Next Gen 5/7-nm RHBD Technology	*Next Gen Demo 5/7nm TRL-6*					
RH Stand Alone Components	Development of Specialty High Performance RH products for use by DoD *SRH Processor Design Complete*		*Fully qualified Components: SRH Processor (100x performance) SRH Memory Products (256 Mb (non-volatile) to 1 Gb (volatile), TRL-8*		*Fully qualified SRH FPGA Recognized as key, multiple program need, TRL-8*						
	RH High Voltage Legacy Components Sustainment, Title III										
RH Lab Modernization	Radiation Testing Infrastructure (NSWC Crane) and Coordination via SRHEC *Newly developed equipment/facility to provide capacity to the strategic community to address future strategic rad-hard testing demand signal at the national level.*										

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- **Enhanced Capabilities**
- **Sustainment Activity**
- *Key Milestones*

Major Investments to Modernize and Sustain Radiation Hardened Microelectronics

Future RH Microelectronics Needs

- Next Generation RHM with greater performance
- Operational Test
- Larger scale and more capacity

Joint Federated Assurance Center (JFAC) Roadmap

Fiscal Years →	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032+
FPGA Assurance	Levels of Assurance (LOA) Development										
	LoA2 Final – Delivered to OUSD	LoA 3 Final Draft	LoA3 Final – Delivered to OUSD								
JFAC Microelectronics Quantifiable Assurance (MQA)	MQA Implementation										
	CIC Pilot Complete		Ramp up JFAC Capabilities to support MQA								
		2 Pilots per Quarter									
	Continuous JFAC Vulnerability Assessment support to Programs										
Supply Chain Awareness	Automated Microelectronics Analysis & Reporting Optimization (AMARO) Tool										
		AMARO Phase 2									
	Attack Countermeasure Analysis (ACMA) Tool										
		ACMA 1.0									
	Supply Chain Analysis Reports and Bulletins										
JFAC Software Assurance	Engineering tools, technical services, best-practices, innovative technologies and other assistance to programs to detect, assess, prioritize, and mitigate software vulnerabilities										

LEGEND

Enhanced Capabilities

Key Milestones

JFAC capabilities provide hardware assurance and vulnerability assessments to ensure the integrity of critical weapon systems

Future JFAC Needs

- Develop COTS Microelectronics Standard
- Continue development of common data analysis tools

Radio Frequency & Optoelectronics (RF/OE) Roadmap

Fiscal Years →	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032+
Material Sources				**RF Gallium Nitride (GaN) Materials**							
		MRL-5 production qualification of new N-Polar GaN material sources with increased capacity and quality		*MRL-6 production demos of N-Polar GaN material for DIB foundries*			*MRL-8 pilot demos of N-Polar GaN material for DIB foundries, enabling max power and efficiency in mmWave devices*				
				MRL-4 R&D demos of SOTA N-Polar GaN foundry capability and devices designs							
GaN Foundry Maturation				**RF GaN Foundry Maturation**							
		MRL-4 R&D demos • *<150nm GaN nodes* • *Advanced Interconnect Study for mmWave*		*MRL-6 production demos* • *<150nm GaN nodes* • *Advanced Interconnects* • *Quantifiable Assurance*			*MRL-8 pilot demos of mmWave RF GaN foundries available to DIB for advanced packaging and integration*				
GaN Device Demonstration				**RF mmWave Device Demonstrations**							
		40nm, 140nm, 150nm RF GaN Device Demos at MRL-4/5 lines		*40nm, 90nm, 150nm RF GaN Device Demos and IP Capture at MRL-6 foundries*			*40nm, 90nm, 150nm RF GaN device demos and IP capture at MRL-8 foundries enabling next generation radar, electronic warfare (EW), and communications*				
Silicon Photonics (SiPh) Foundry Maturation				**SiPh Foundry Maturation**							
		Demonstrate early access to SOTA SiPh nodes and develop maturation plan					*Demonstrate open foundry access to mature SOTA SiPh nodes*				
							Mature SOTA SiPh foundry capability and capacity for next generation radar, EW, and communications				
SiPh Device Demonstration				**SiPh Device Demonstration**							
		Demonstrate open access designs at AIM and GF 45SPCLO			*Datacom and EW prototype designs, which enable new warfighter capabilities and enhanced SWAP*			*RF Optical Transceiver SHIP Demonstrator*			

LEGEND

Enhanced Capabilities

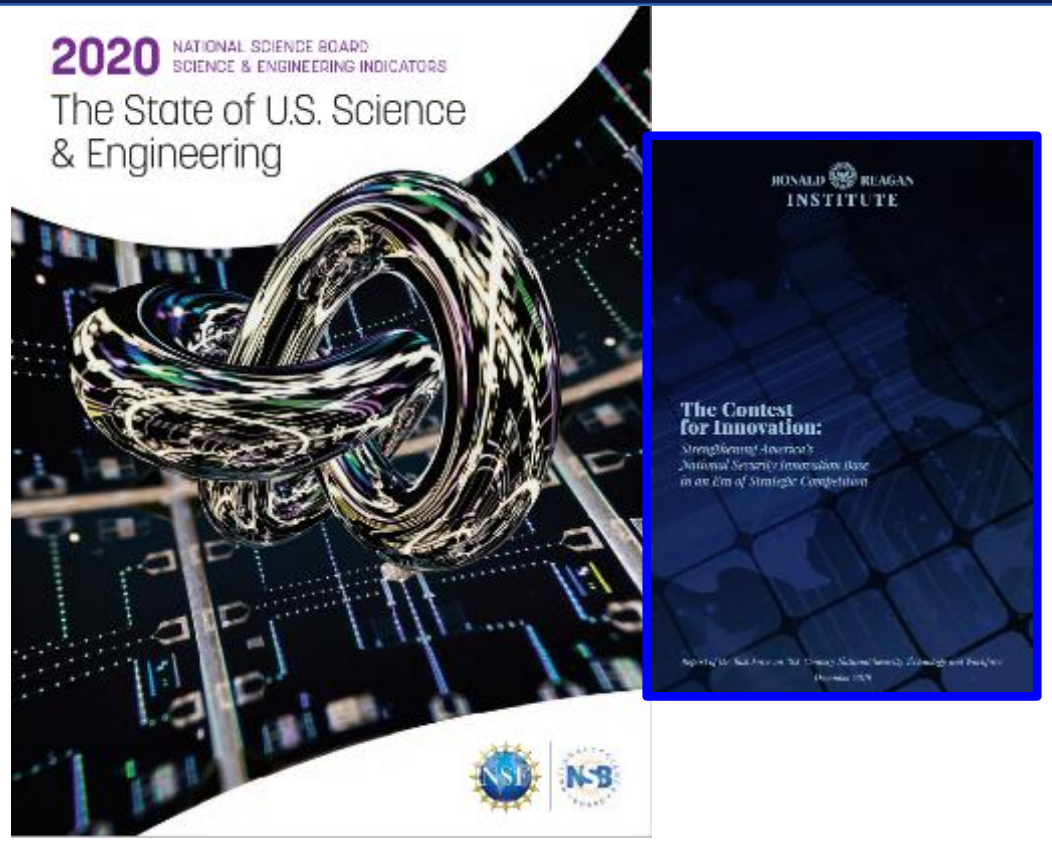
Key Milestones | *Unfunded Option*

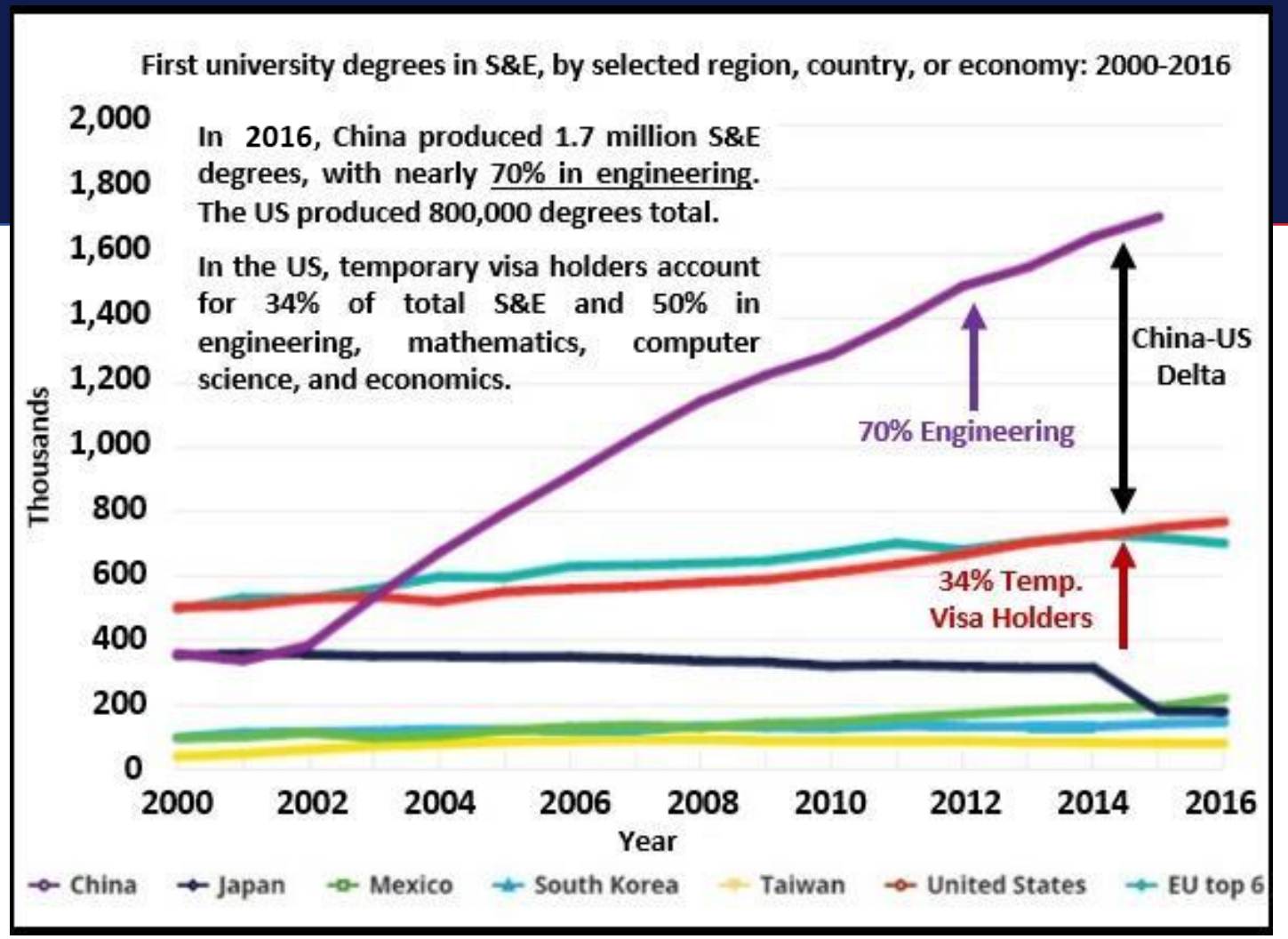
Major Investments to Mature the Domestic SOTA RF/OE Microelectronics Ecosystem

Future RF/OE Microelectronics Needs

- Domestic access to mature SOTA RF/OE materials, foundries, and packaging
- Ecosystem alignment to DIB and POR

STEM Talent Crisis





As much as emerging technologies will define future conflict, ***the war for talent will likely play the central role*** in the outcome of long-term technological competition.

The National Security Innovation Base (NSIB) struggles to attract, recruit, and retain a workforce willing and able to tackle tough challenges and find innovative solutions. Universities are confronting a dearth in American talent generation and retention. Much of that shortfall is filled with foreign students, a large share of them from China.

Education and Workforce Development Roadmap

Fiscal Years →	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032+
Establish & Maintain Technology-Specific Consortia											
	Scalable Asymmetric Lifecycle Engagement (SCALE)										
	Create / Update / Teach Targeted Curricula; ID & Perform Research; Recruit Students; Facilitate Internships; Students Graduate (Repeats every year)										
	National Microelectronics Security Training Center (MEST)										
	Develop and provide training programs on microelectronics design and security to the Government and Defense Industrial Base (Repeats every year)										
Enable DoD-Specific Challenges & Training											
	Needs Assessment, Community College Engagement Exemplar										
	System Engineering and Dynamics for Services (NPS, AFIT)										
	Students focus on Microelectronics and supply chain issues (Repeats every year)										

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Enhanced Capabilities

Key Milestones

Attract, Develop, and Maintain a Ready Workforce

Future Education & Workforce Dev Needs

- Additional funding/capacity
- Ways to leverage veterans
- Awareness / Integration with AFRL, AFWERX, other DoD capabilities

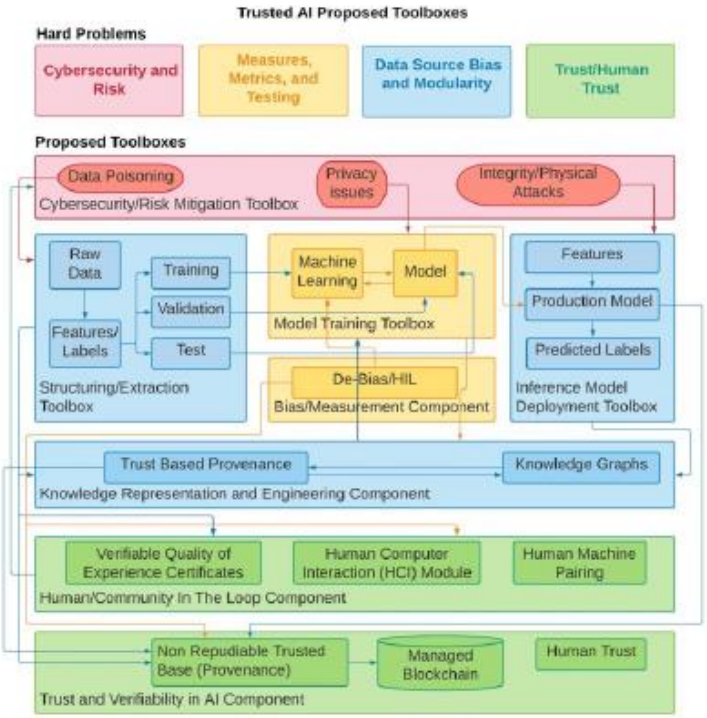
Scalable Asymmetric Lifecycle Engagement (SCALE) TOPIC AREAS with HWA Components

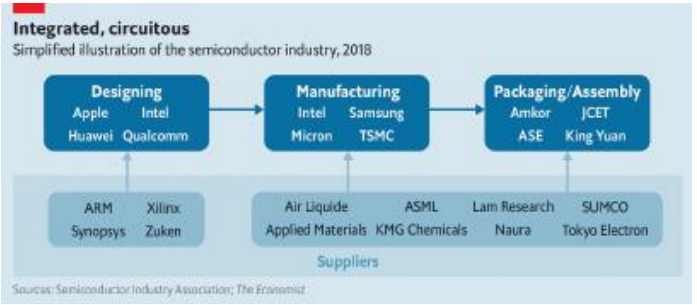
Artificial Intelligence (AI)

- Artificial intelligence (AI) provides a tremendous amount of sophisticated information analysis and decision making capabilities
- AI has even been characterized as a potential third offset for DOD, if it can be trusted
- Trusted AI requires addressing hard challenges such as verifiability, bias, fairness, explainability, and human interaction and feedback

Supply Chain Awareness

- With the increasingly central role of electronic hardware in a broad range of defense applications, securing supplies of electronics is more important than ever before.
- At the same time, exponential growth and complexity in semiconductor manufacturing creates potential supply chain disruption at all levels
- Challenges include understanding potential risks of IP security, measuring and detecting potential tampering with manufacturing and packaging, as well as improving supply chain resilience



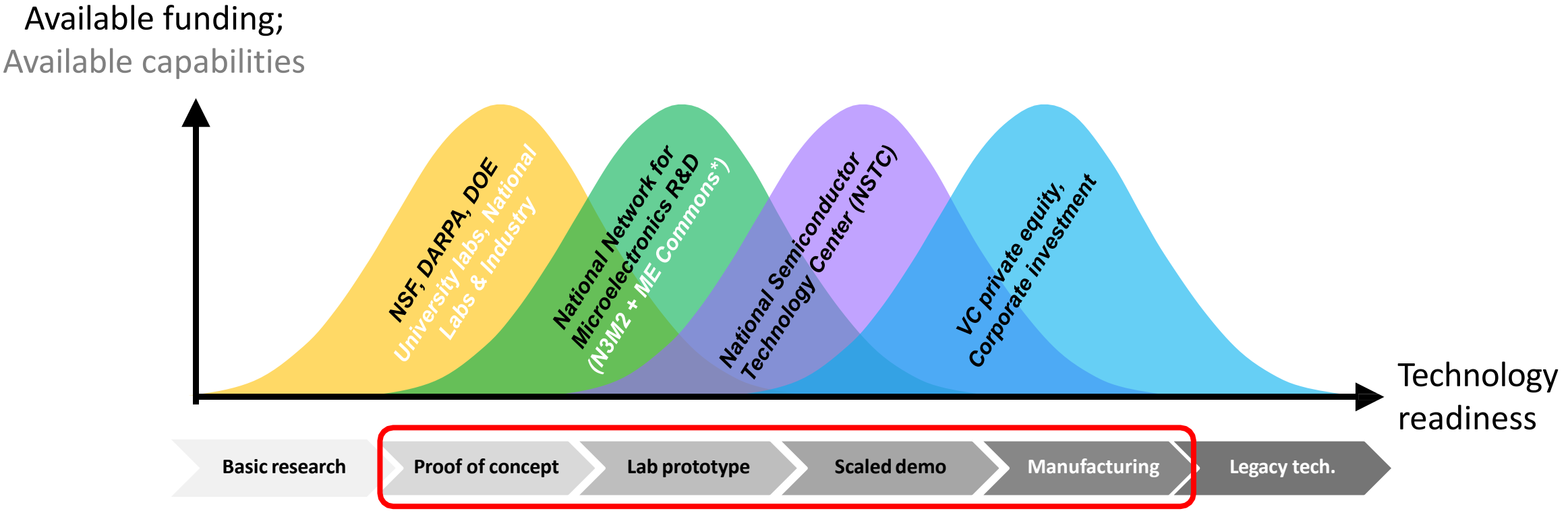


Other Scale Topic Areas Include: Radiation Hardened Microelectronics, SoCs and Advanced Packaging/Heterogeneous Integration

National Network for Microelectronics R&D: Ideation to Commercialization

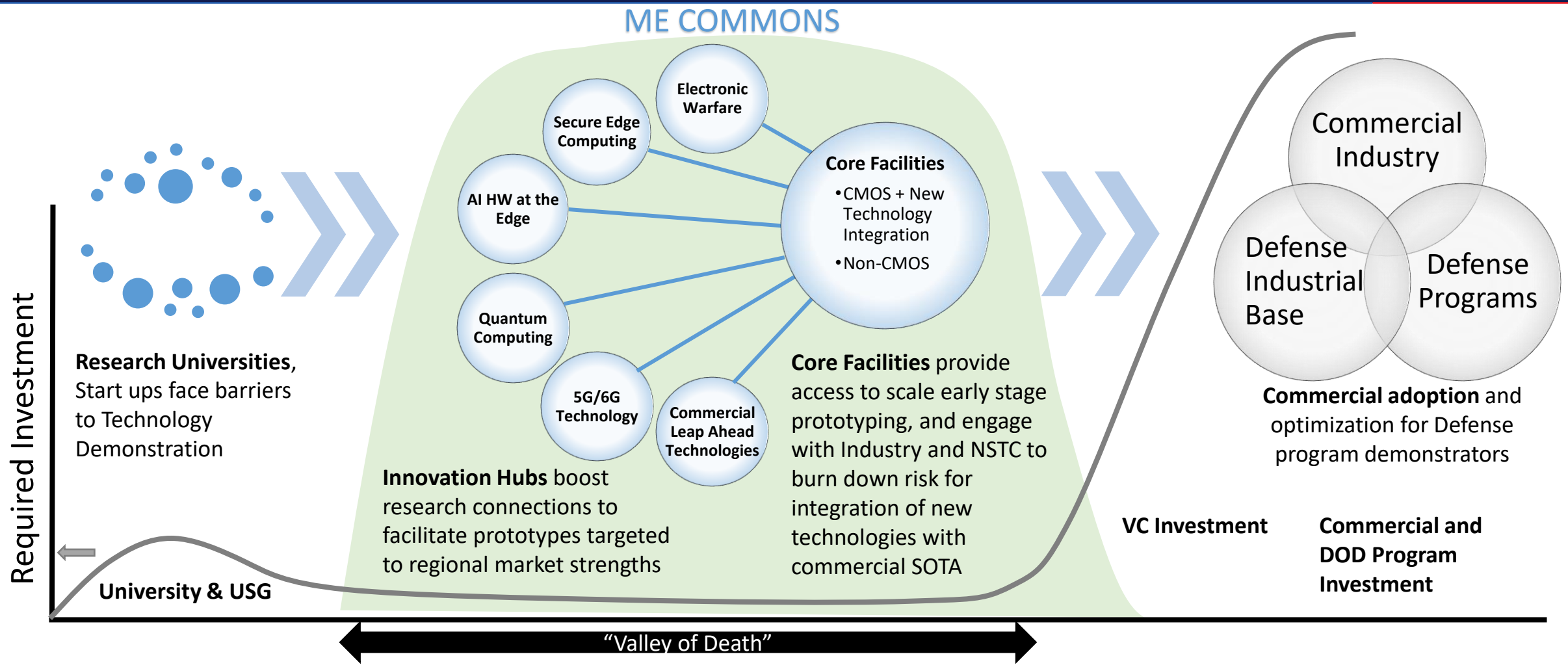
Mission

- **Cost-effective exploration of chip-scale and package-scale systems in domestic facilities**
- **Accelerate transition of new technologies to domestic microelectronics manufacturers**



Adapted from : White paper on "Microelectronics Commons," V. Coleman, Z. Holman, T.-J. King Liu, K. Squires, H.-S. P. Wong (2020)

Microelectronics Commons Addresses the Valley of Death



Salient Points

- DoD faces many challenges for secure, low cost access to extant systems, state of practice, and leading edge
  - Aggregation of microelectronics demand across critical sectors provides an opportunity for DoD and partners
- DoD has developed roadmaps for secure access to critical technologies including:
  - SOTA microelectronics
  - Advanced packaging and testing
  - Joint Federated Assurance Center (JFAC) Roadmap
  - Educational and Workforce Development Roadmaps
- DoD and the interagency are planning for CHIPS funding related investments